AMERICAN UNIVERSITY OF BEIRUT

# A NEW MILLIMETER WAVE PHASE SHIFTER FOR PHASED ARRAYS

by
MICHELLA BOUTROS RUSTOM

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AMERICAN UNIVERSITY OF BEIRUT

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"I have come so that they may have life and have it to the full." (John 10:10)

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# AN ABSTRACT OF THE THESIS OF

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Title: A New Millimeter Wave Phase Shifter for Phased Arrays

Phase shifters are considered crucial functional blocks in electronically scanned arrays, governing their beam steering capabilities. They are used to adjust the phase of each antenna element in the array and electronically steer the main lobe of its radiation pattern in the desired direction. Featuring components' compactness and large available bandwidth, the mm-wave frequency band, particularly the unlicensed 57-64 GHz ISM band, is an attractive band for the design of phase shifters for phased array systems, which are implemented using low cost silicon-based processes.

The aim of this thesis is to present the design of a new millimeter wave phase shifter for phased arrays, which is envisioned to be employed in high-resolution sensing applications. A reflective-type phase shifter is chosen and designed to operate at 60 GHz due to its simple design and controlling scheme. The design is implemented in the 90nm industrial CMOS technology using Cadence Virtuoso platform and Ansys HFSS 3-D layout. It involves a new topology for a fourth order asymmetric reflective load which is composed of two AMOS-based varactors and two inductors. Overall, the reflective type phase shifter is capable of achieving a maximum phase range of 254° with a low insertion loss, resulting in a high figure of merit of around 22°/dB. It is also characterized by high linearity and a low DC power consumption of approximately 25 $\mu$W.

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# ABBREVIATIONS

ADE: Analog Design Environment

AED: Ansys Electronics Desktop

AMOS: Accumulation mode MOS varactor

BEOL : Back End Of Line

BPF: Band Pass Filter

BST: Barium Strontium Titanate

CMOS: Complementary Metal-Oxide Semiconductor

D=B=S: Drain connected to Body connected to Source

dB: Decibel

DBF: Digital Beamforming

DC: Direct Current

DRC: Design Rule Check

DUT: Device Under Test

EIRP: Effective Isotropic Radiated Power

EM: Electro Magnetic

EsoA: European School of Antennas

FEOL : Front End Of Line

FFT: Fast Fourier Transform

FMCW: Frequency-Modulated Continuous-Wave

FoM: Figure of Merit

GaAs: Gallium Arsenide

HFSS: High Frequency Structure Simulator

HPBW: Half Power Beam Width

Hz: Hertz

IC: Integrated Circuit

IDC: Interdigital Capacitor

IETR: Institute of Electronics and Telecommunications of Rennes

IF: Intermediate Frequency

ILD: Inter-Layer Dielectric

IMD: Inter-Metal Dielectric

IMOS: Inversion-mode MOS varactor

InP: Indium Phosphide

ISM: Industrial, Scientific and Medical

LTCC: Low temperature co-fired ceramics

LVS: Layout Versus Schematic

MEMS: Micro-Electro-Mechanical Systems

MIM: Metal-Insulator-Metal

MMIC: Monolithic Microwave Integrated Circuits

mm-wave: Millimeter wave

MOS: Metal Oxide Semiconductor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Mx: Metal x

NMOS: Negative Channel Metal-Oxide Semiconductor

O.C.: Open-Circuit

PCB: Printed-Circuit Board

Pcell: Parameterized cell

PE: Parasitic Extraction

PEX: Parasitic Extraction using XCalibre

PIN: Positive-Intrinsic-Negative

PMOS: Positive Channel Metal-Oxide Semiconductor

PS: Phase Shifter

Q-factor: Quality factor

RF: Radio Frequency

RFIC: Radio Frequency Integrated Circuit

RL: Return Loss

RMS: Root Mean Square

RTPS: Reflective-Type Phase Shifter

S.C.: Short-Circuit

SiGe: Silicon Germanium

SLLs: Side Lobe Levels

SOI: Silicon On Insulator

S-Parameters: Scattering Parameters

SPDT: Single Pole Double Throw

T-line: Transmission line

UTM: Ultra-Thick Metal

VCO: Voltage-Controlled Oscillator

VM: Vector Modulator

*To my beautiful village in northern Lebanon: Memneh, Akkar*

*To my parents, Boutros and Antoinette*

*To my brother, Alexios*

# CHAPTER 1

# INTRODUCTION

Despite high propagation loss and atmospheric attenuation, the millimeter-wave frequency range, particularly the unlicensed 57-64 GHz ISM bands, offers high transmission power levels, smaller antenna size and high data rates. In this context, the design of mm-wave enabled devices and circuits has become useful and highly relevant to many modern applications such as automotive radars, sensor systems, high-data rate wireless communication systems and active/passive imaging systems [1, 2].

A crucial component in many communication systems is the RF phase shifter. At mm-wave frequencies, traditional PCB based phase shifters lack the required specifications, hence silicon-based technologies are sought. In fact, low-cost silicon based technologies, such as CMOS and SiGe semiconductor technologies, are employed in implementing RF phase shifters, especially at millimeter-wave and terahertz frequencies.

In this thesis, the design of a new millimeter wave phase shifter for phased arrays is presented and envisioned to be used in high-resolution sensing applications as a crucial block in the phased array feeding network. A reflective-type phase shifter (RTPS) is designed at 60 GHz and implemented in the 90 nm industrial CMOS technology using Cadence Virtuoso platform [3] and Ansys Electronics Desktop (ADE) HFSS 3-D layout [4]. It is composed of two main blocks: a 3-dB hybrid coupler and two identical reflective loads terminating both the through and the coupled ports of the coupler. A new asymmetric $4^{th}$ order topology is chosen for the reflective load,

employing two AMOS-based varactors and two inductors. Overall, the reflective-type phase shifter is capable of achieving a maximum phase range of 254° with a low insertion loss, resulting in a high figure of merit of around 22°/dB. It is also characterized by high linearity and low DC power consumption of ~ 25 $\mu$W.

Chapter 2 of this report presents a literature review of the state-of-the-art research on phased antenna arrays.

Chapter 3 provides a review of the state-of-the-art research on phase shifters as key components in achieving the beam steering capability of phased antenna arrays.

Chapter 4 reviews RFIC design basics for a phase shifter implementation with focus on CMOS technology due to its low-cost and high-performance characteristics.

Chapter 5 presents a software control solution implementation for back end circuitry in order to extract the scattering parameters from measurement devices or antenna arrays components.

Chapter 6 presents a four-element linear phased array at microwave frequencies. Its aim is to validate the ability to beam steer the array radiation pattern; a previously studied phased antenna array network is tested along with its phase shifters.

Chapter 7 details a newly proposed millimeter wave reflective-type phase shifter design. It is composed of a 3-dB hybrid coupler as well as a novel reflective load with AMOS-based varactors.

Chapter 8 summarizes the thesis work and highlights future plans that are envisioned to be completed.

# CHAPTER 2

# PHASED ANTENNA ARRAYS

## 2.1 Introduction

Phased antenna arrays [5-7] are antenna arrays that are composed of a number of radiating elements fed by a network that employs appropriate phase shifts between the various elements. As a result, the array's main beam is steered to the desired direction.

Phased arrays are composed of three main blocks: a power distribution network, a weighting board including phase shifters and attenuators, and the radiating antenna array. In this context, the feeding network in the phased-array design plays an important role in achieving the beam steering. In general, the array field pattern for a given array consisting of identical elements is the multiplication of the individual element field pattern by the array factor. The latter depends on the array geometrical configuration (linear, rectangular, triangular, etc.), the distance between the antenna elements as well as the amplitude and phase excitations of the individual elements. Note that the main radiation lobe can be directed to the desired direction by controlling the phase excitation between the elements, and the side lobe levels (SLLs) are controlled by appropriately tapering the excitation amplitude distribution.

Phased-array systems find their applications in many areas such as defense and satellite communication systems for high-data rate communications, radio astronomy, optics, etc. [1, 2, 8-10]. These applications require narrow beams with low SLLs that are

able to scan a wide field of view. On the other hand, in the past few years, electronically scanned arrays have been utilized in commercial applications such as automotive radars, landing systems and advanced robotic sensors, which necessitate a narrow field of view with low cost and low complexity criteria.

## 2.2 State of the Art

In this section, a review of the state of the art applications of phased arrays is presented. Many challenges arise in the design of phased array systems such as the complexity of the feeding network, beamsteering approaches, and transceiver designs at millimeter-wave and terahertz frequencies on a single chip, among others.

### *2.2.1 Alleviating Feeding Network Complexity*

A new phased-array feeding network is presented in [11] in order to improve the scanning performance of limited-scan arrays without using a complex feed network. In this design, the individual phased-array elements are grouped into random sequences of nonuniform subarrays and each subarray employs a single phase shifter. This random grouping is optimized in order to result in the largest scan-angle with grating lobes less than a desired limit. A 1-D random array is fabricated at 7.9 GHz for 30-element linear design (four series-fed antenna element scanning in one direction) with 12 PSs, resulting in a half power beam width (HPBW) of 4.1° with a scan angle up to $\pm 14°$ and SLLs less than -15 dB as shown in Figure 2.1 & 2.2. Compared to the conventional uniform subarrays where identical primary arrays are used, it is shown that the 1-D random arrays reduce the number of phase shifters by 40% while preserving the same performance. It is also shown that, for the same performance, 2-D random arrays reduce

the number of phase shifters (PSs) by up to 60% compared with uniformly grouped 2-D arrays. The suggested design finds its application in low-cost phased arrays with limited scan angles such as automotive radars or landing systems [11].

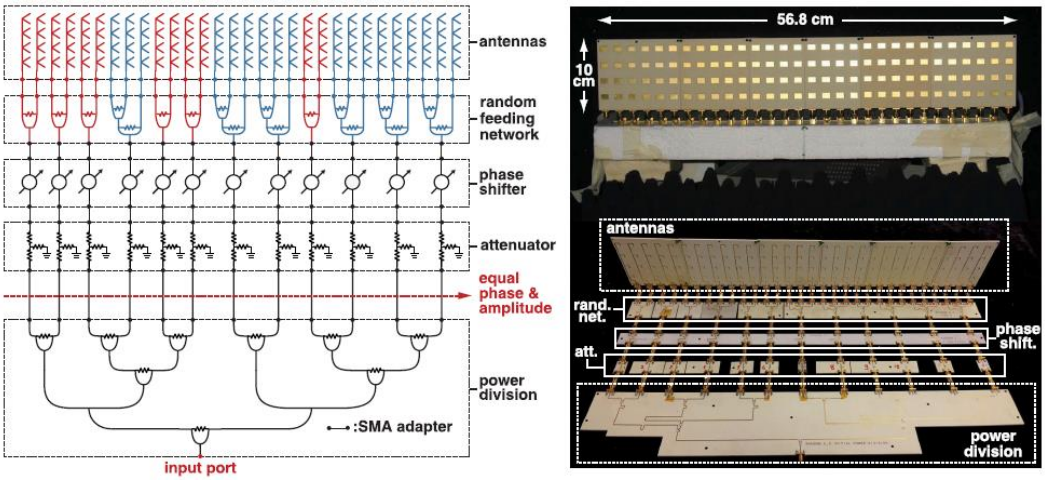


**Figure 2.1: Random array schematic and its fabricated prototype [11].**

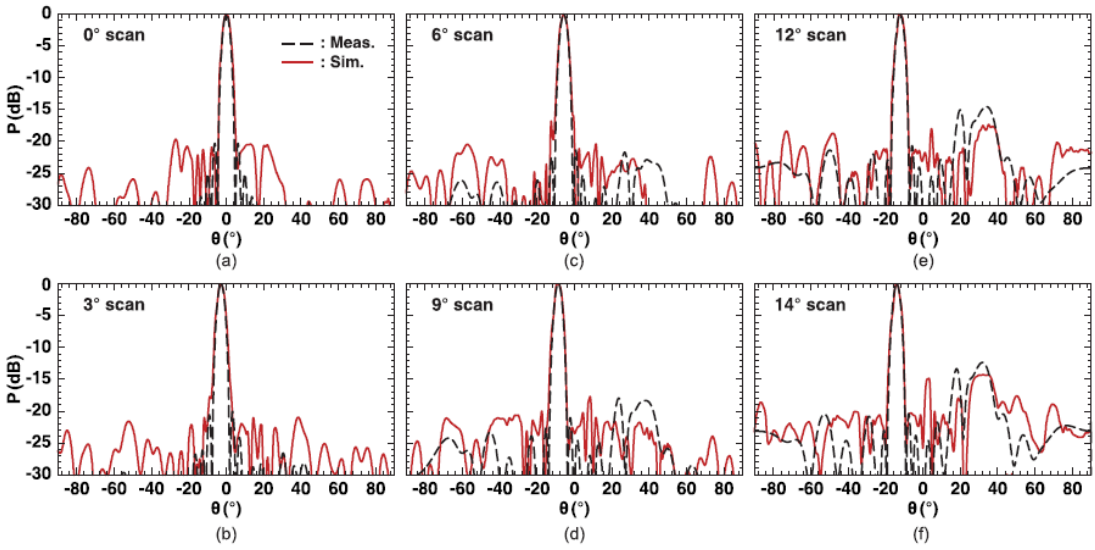


**Figure 2.2: Normalized measured and calculated radiation patterns versus θ for (a) 0°, (b) 3°, (c) 6°, (d) 9°, (e) 12°, and (f) 14° scans [11].**

Another phased-array feeding network is presented in [12], where a multiport interwoven feeding network is employed. In this network, each phase shifter feeds all of the antennas in the array by relying on unit cells that consist of hybrid couplers, Wilkinson power dividers and resistive attenuators [12]. Two prototype linear arrays with 28 elements (four series-fed antenna elements) operating at 7.9 GHz are presented, where the first array employs 14 PSs, as shown in Figure 2.3 and 2.4, and is able to scan up to $\pm 24°$. The second array employs 7 PSs and is able to scan up to $\pm 11°$. Both of these arrays reach a HPBW of 4° with SLLs less than -15 dB. They show state-of-the-art performance in terms of reducing the number of phase shifters while resulting in low SLLs over the entire scan region. In fact, interwoven arrays constitute a promising approach for implementing larger subarrays and reducing the number of PSs in limited-scan arrays as detailed by [12]. An approach for further reducing the SLLs is also presented by replacing the straight vertical antenna cells in an array by zig-zag antenna cells in order to result in a triangular lattice.

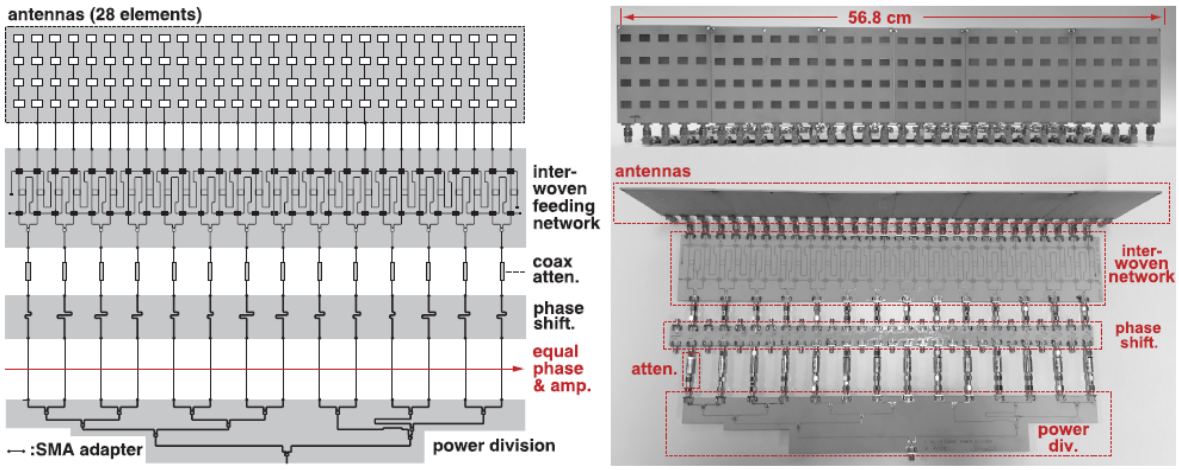


**Figure 2.3: Interwoven array schematic and its fabricated prototype with 28 elements and 14 PSs [12].**

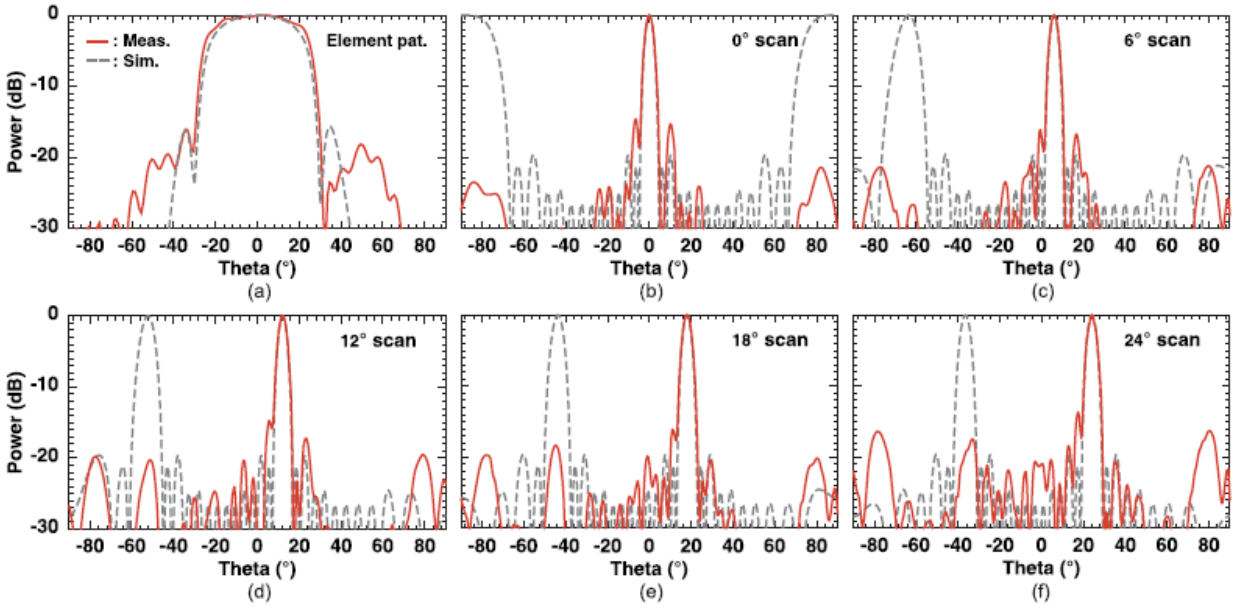


**Figure 2.4: (a) Simulated and measured normalized element patterns of the 1:2 array at 7.8 GHz. Measured radiation pattern of the 28-element 1:2 array and the simulated grating lobes at (b) 0°, (c) 6°, (d) 12°, (e) 18°, and (f) 24° scans [12].**

### *2.2.2 Beam Steering Approaches*

A novel approach to beam steering is introduced for 1-D and 2-D scanning arrays in [13, 14]. The approach is based on introducing antenna arrays that are capable of supporting multiple radiating modes. Such approach reduces the unwanted mutual coupling and increases the array scan range. However, this comes at the expense of increase in the physical size.

Figure 2.5 shows a fully assembled 16-element hybrid phased array (four four-element multiple mode dipole subarrays) [13] operating at 4.6 GHz. Each subarray is fed by an active feed board that has a unique hardware defined address and contains four low noise amplifiers (LNAs), four digital step phase shifters (DPS), four digital step attenuators (DAT), and other supporting circuitry. The combined RF output of each

active feed board is connected to a final Wilkinson power combiner and then routed to the VNA receiver for measurement.

Figure 2.6 shows a hybrid phased array (2 × 2 × 3) [14] consisting of four patch antennas each with two feed points. Additional collocated active monopole elements are also integrated on the respective patches [14]. This proposed design is compared with the conventional patch antenna array (2 × 2 × 2) and the conventional array (3 × 3 × 2). Measured data of the hybrid phased array demonstrates an improved scan range that reaches $\pm 50°$.

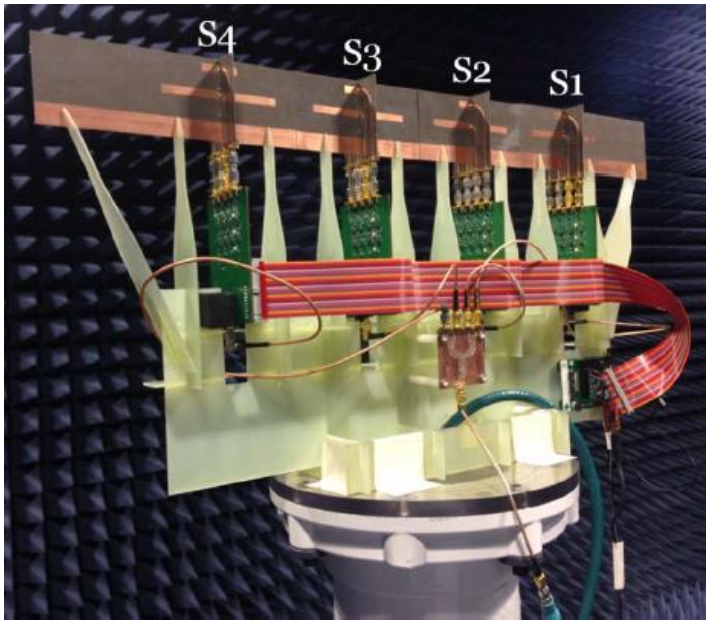


**Figure 2.5: Fully assembled 16-element hybrid phased array with active feed networks as mounted in the anechoic chamber [13].**

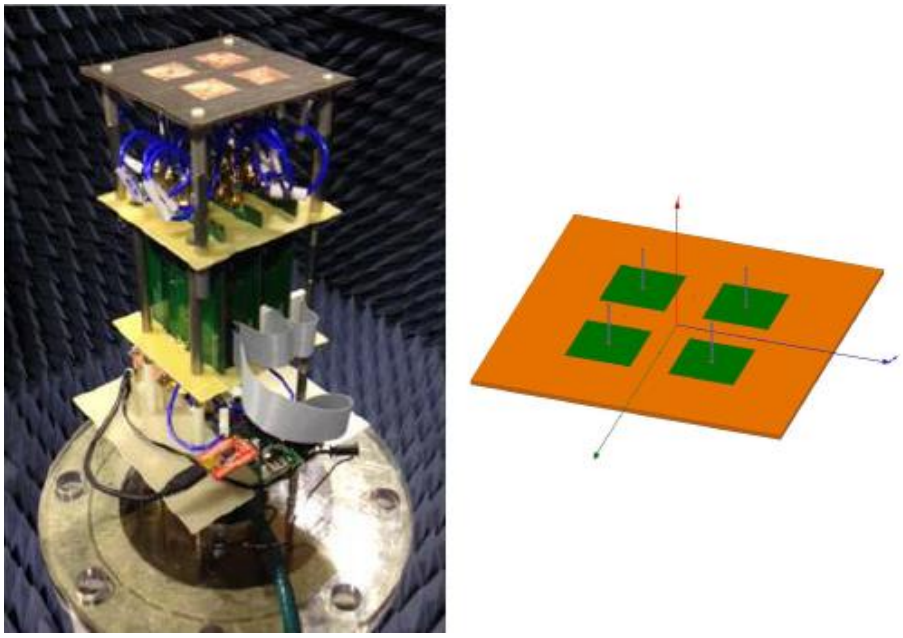

**Figure 2.6: Patch and monopole array (m × n × p) = (2 × 2 × 3) with λ/2 interelement spacing where m is the number of unit cell locations along the x-axis, n is the number of unit cell locations along the y-axis, and p is the number of feed points at each location [14].**

### *2.2.3 Mm-wave and Terahertz Phased-Array Transmitter/Receivers*

In recent years, the use of CMOS and SiGe BiCMOS [15] technologies employed for RF and digital beamforming (DBF) phased array systems has been a flourishing and extremely challenging research area, especially when it comes to the design of millimeter-wave and terahertz transmitters and receivers.

A 16-element linear microstrip phased-array receiver, based on a single SiGe chip with RF beamforming capabilities and packaged using low-cost bond-wire techniques as shown in Figure 2.7 & 2.8, is presented in [16] for advanced W-band automotive radars. Its directivity reaches 29.3 dB with fine beam scanning capabilities up to $\pm 50°$ in the azimuth plane in $\sim 1°$ steps. It is also employed with a 2-element

FMCW transmitter at 76.5–77 GHz, which yields high-resolution millimeter-wave radar data and images taken on cars and pedestrians.

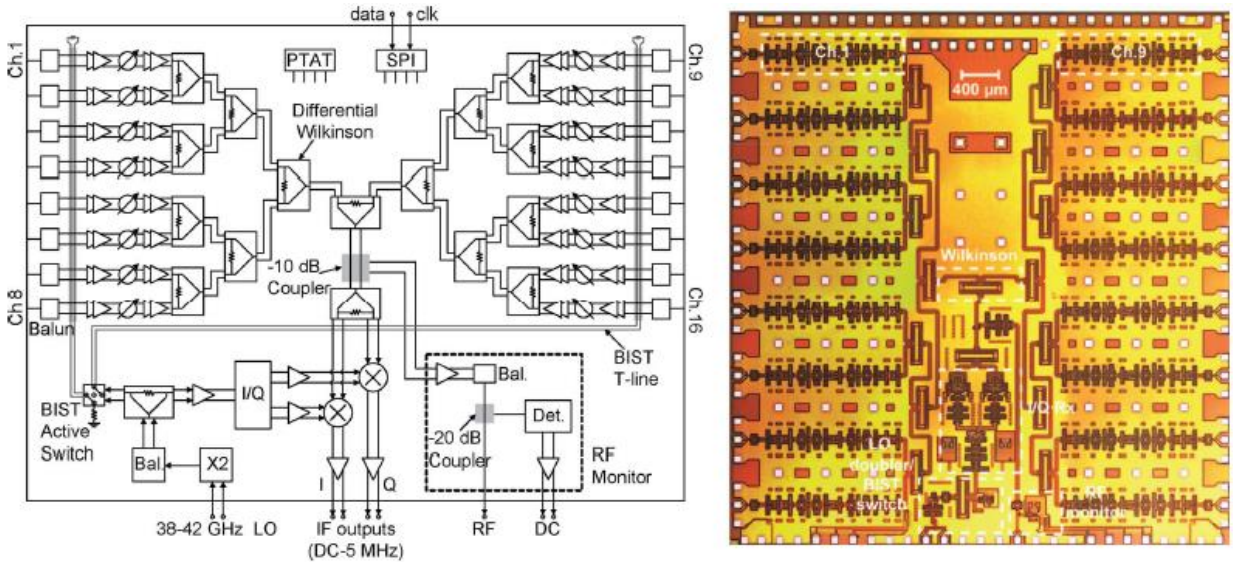


**Figure 2.7: Block diagram of the 16-element receiver chip and its microphotograph (5.5 × 5.8 $mm^2$) [16].**

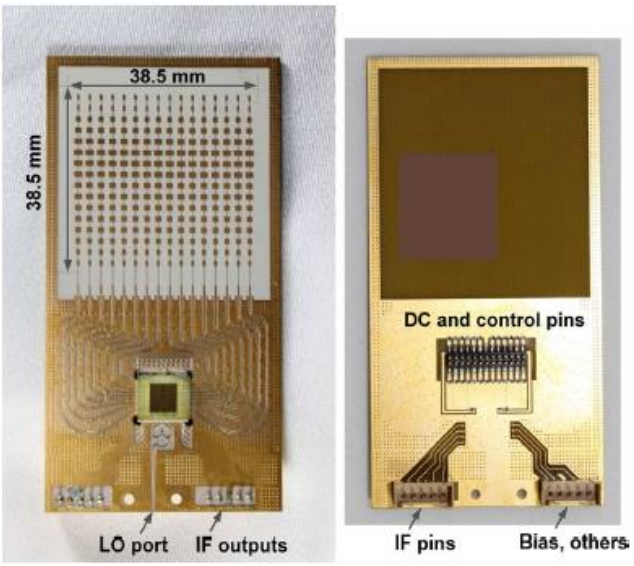


**Figure 2.8: 16-element phased array including antennas and LO rat-race coupler. IF and digital control are on the back side of the board. The antenna size is 38.5 × 38.5 $mm^2$ [16].**

As shown in Figure 2.9, a 60-GHz wafer-scale phased array transmitter with 64- and 256-elements is presented in [17] using full-reticle and sub-reticle stitching techniques respectively. A 1-4 Gb/s communication system using the 64-elements phased array is demonstrated to be able to scan up to $\pm 45°$ in the E- and H-planes at 4-, 30-, and 100-m ranges. It represents the first demonstration of large size (64- and 256-element) phased-array transmitters on a single wafer.

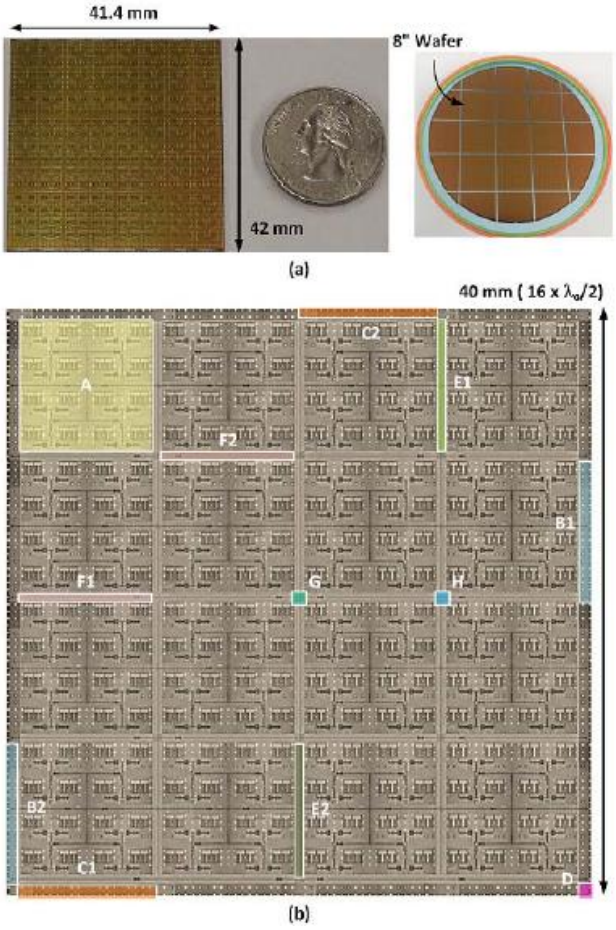


**Figure 2.9: (a) Photograph of the fabricated 256-element phased array on a 200-mm wafer with a quarter and (b) expanded view showing the different sub blocks used [17].**

A 370-410 GHz eight-element linear phased-array transmitter is presented in [18] which is built using 45-nm CMOS silicon on insulator technology. As shown in Figure 2.10, the feeding network consists of a W-band distribution network, W-band phase shifters (VM) and amplifiers coupled with ×4 multipliers for frequency up conversion and with on-chip high efficiency microstrip antennas. The transmitter is able to operate over a 30 GHz bandwidth with an EIRP > 5 dBm and a peak EIRP of 7–8 dBm at 380-400 GHz. The system performance results in a phased-array pattern scanning to $\pm$ 35° in one plane. This design is considered to be one of the first demonstrations of a phased antenna array operating at 400 GHz using CMOS technology. It is also the first to operate over a wide bandwidth, and with scalability as a prime design factor.

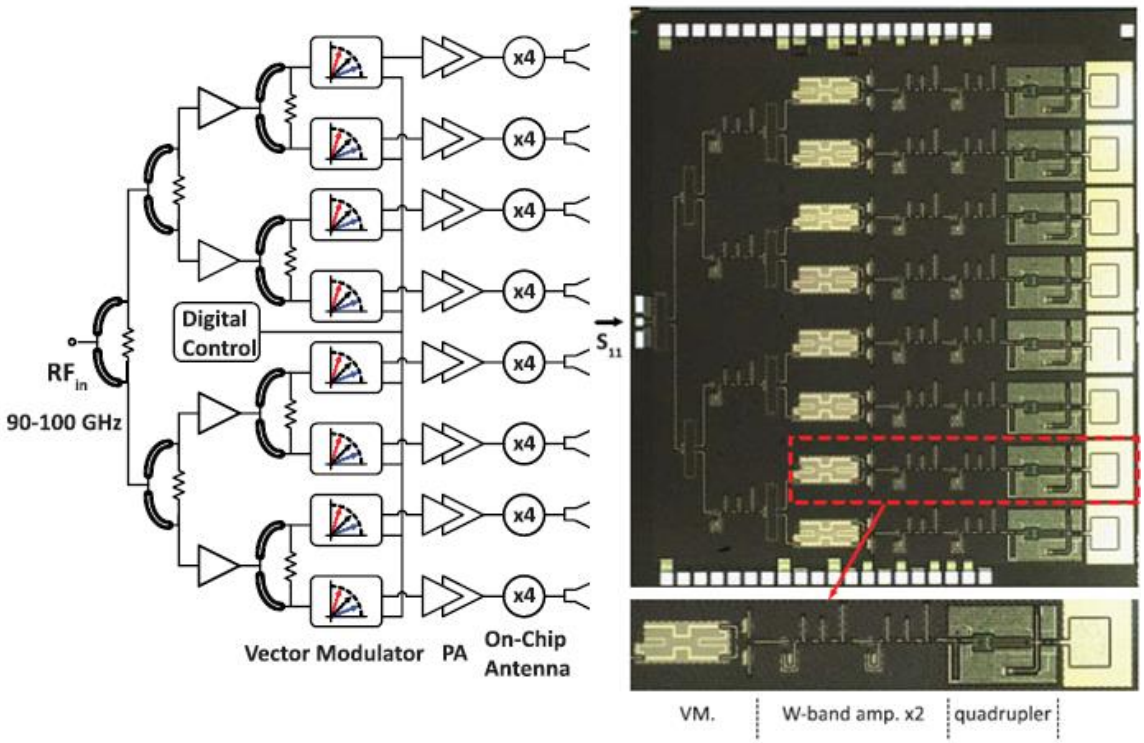


**Figure 2.10: Block diagram of the 400 GHz phased-array transmitter and its microphotograph ($3 \times 3.5\ mm^2$) [18].**

## 2.3 Discussion

In this chapter, phased antenna arrays in the literature are presented. Several challenges arise in the design of phased arrays, such as the need for scaled designs with less complexity. Newly proposed beamsteering approaches that feature improved scan range, involving multiple radiating modes are also discussed. Finally, millimeter-wave and terahertz phased-array transmitters and receivers, implemented in CMOS and SiGe BiCMOS technologies, are reviewed.

# CHAPTER 3

# PHASE SHIFTERS

## 3.1 Introduction

Phase shifters are considered crucial functional blocks in electronically scanned arrays, governing their beam steering and beam forming capability. In fact, they are able to adjust the phase of each antenna element in a given array and steer the array's main lobe in the desired direction as shown in Figure 3.1.

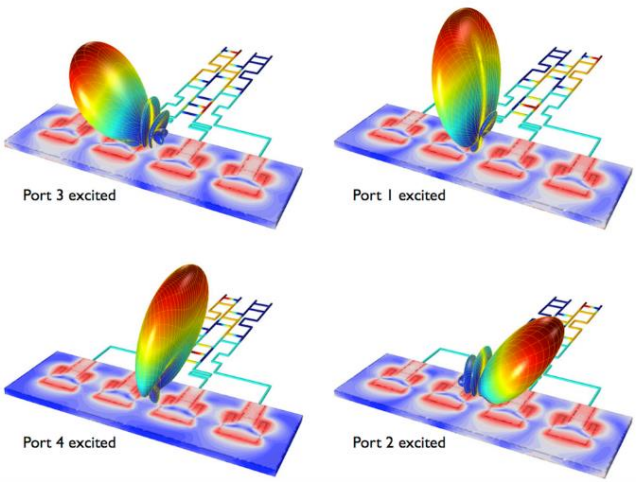


**Figure 3.1: Phase shifters as functional blocks in phased-array system [19].**

In general, the scattering parameters of an ideal PS are given as follows:

$$\mathbf{S} = \begin{bmatrix} 0 & |S_{21}|e^{-j\varphi} \\ |S_{21}|e^{-j\varphi} & 0 \end{bmatrix}$$

where $|S_{21}|$ is the gain of the PS and $\varphi$ is the applied phase shift. Both parameters vary as function of the frequency.

Phase shifters can be classified into different categories depending on the type of phase shift control, frequency dependency, and underlying component complexity.

RF phase shifters can be classified into two different categories depending on the phase shift control: digital or analog. In digital phase shifters [20], multi-bit phase shifters are implemented using multiple stages of fixed phase shift that are cascaded and controlled by control bits using switches. They are characterized by fairly good linearity. However, they suffer from high losses due to the use of switches, and do not provide continuous phase shifting. Such performance results in high-SLL in the array radiation pattern. On the other hand, analog or continuous PSs vary the phase in a continuous way for a certain range by setting the control voltage to the appropriate value.

Based on the frequency dependence of the phase shift, RF phase shifters can also be classified into two categories:

- Constant phase type: applies a constant phase shift over the frequency band i.e. $\varphi(\omega) = \varphi_0$.
- Constant time delay type: also named true time delay (TTD), applies a constant time delay $\varphi(\omega) = \omega\Delta t$, where the phase varies linearly with respect to the frequency. Usually a time delay unit does not have variable phase shift unless switches are used, which increases the overall cost of the system.

RF phase shifters can also be classified as active or passive phase shifters [21]. Active phase shifters [22], such as vector modulator PSs, provide high gain and high phase accuracy; however, they suffer from high DC power consumption and complex digital control circuits. On the other hand, passive phase shifters, such as the reflective-

type PS, present better noise characteristics with simple circuitry. These PSs do not consume DC power consumption, have better linearity and lower control complexity. Hence, they are essential in large-scaled and power-constrained phased array transceivers.

## 3.2 Design Metrics

Common requirements in the design of a variable phase shifter over the desired frequency band are the following [23]:

- Large phase-control range
- Small phase-shift step size for digital phase shifters
- Low insertion loss
- Low insertion loss variation over all phase states
- Low power consumption and small chip area
- Wide bandwidth for broadband beam steering (RMS phase and amplitude errors) [24]

Most importantly, to be able to differentiate between phase shifters employing different topologies and underlying technologies, the overall performance of a given phase shifter is evaluated by the following Figure of Merit (FoM) defined as follows:

$$FoM = \frac{\Delta\varphi_{max}}{IL_{max}}$$

where $\Delta\varphi_{max}$ is the maximum differential phase shift and $IL_{max}$ is the maximum insertion of the phase shifter [25].

## 3.3 Common Topologies

In this section, some common topologies of phase shifters are presented with their corresponding characteristics: switch-type, loaded-line, and reflective-type phase shifters.

### *3.3.1 Switch-Type Phase Shifter*

A switch-type phase shifter can be achieved by using either switched T-lines or high-pass/low-pass signal paths as shown in Figure 3.2. A difference in the electrical lengths between the T-lines produces this phase shift. This type of phase shifter is used to achieve large phase shift steps (90º and 180º). The choice of SPDT switches ranges from PIN diode switches to transistor-based switches to MEMS devices [23].

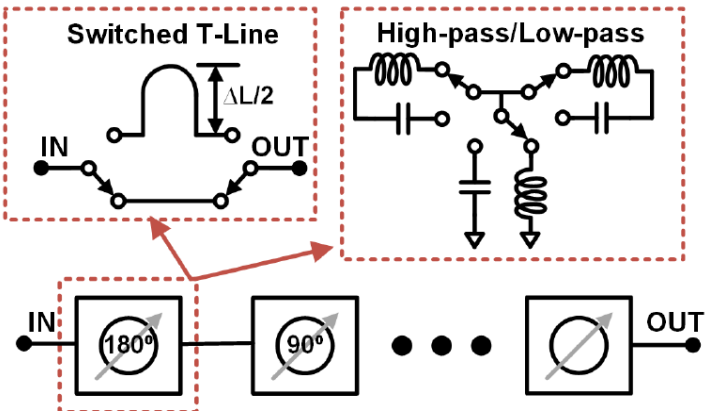


**Figure 3.2: Switch-type phase shifter topology [26].**

### *3.3.2 Loaded-Line Phase Shifter*

In this type of phase shifter, the transmission line is loaded with reflective loads, i.e. fixed inductors (usually lumped inductors or distributed transmission line) and tunable capacitors. As a result, the incident wave undergoes a certain phase shift as shown in Figure 3.3. The capacitance values are varied by using MOS semiconductor based varactors or switching capacitors, hence creating some perturbation in the phase of the signal, while minimizing the amplitude perturbation. In fact, a large phase control range can be achieved by making the electrical length of the distributed transmission line equal to 90°, since the capacitance control ratio $\frac{C_{max}}{C_{min}}$ is usually limited. Note that this type of phase shifters is used to achieve phase shift steps of 45º or lower [23].

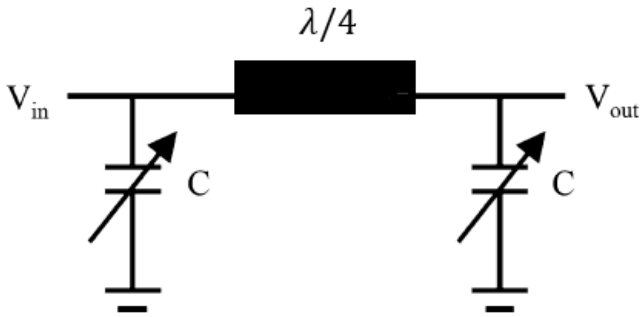


**Figure 3.3: Loaded-Line Phase Shifter Topology.**

### *3.3.3 Reflective Type Phase Shifter*

An RTPS consists of a 3-dB 90° hybrid coupler terminated with two identical reflective loads at ports 2 and 4 as shown in Figure 3.4. The input signal at port 1 is reflected to the output at port 3 with some phase shift which can be controlled by appropriately tuning the reflective loads. In other words, matching is maintained at both the input and the output, and the transmission coefficient becomes identical to the reflection coefficient of the reflective loads with some phase offset. Varying the

impedance of the reflective loads will vary their reflection coefficient, hence the transmission coefficient between input and output, and a phase shifter is realized.

In this thesis, a reflective-type phase shifter operational at 60 GHz is presented with a detailed discussion that follows in Chapter 7.

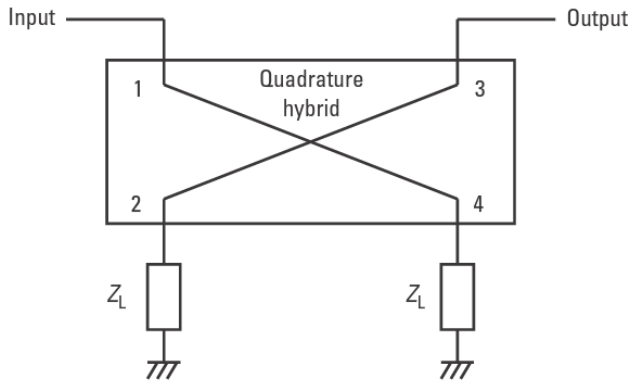


**Figure 3.4: Reflective Type Phase Shifter Block Diagram [27].**

## 3.4 State of the Art

In this section, a review of state of the art phase shifters in literature is presented, in terms of their topologies, characteristics and the underlying technologies.

### *3.4.1 Loaded-Line Phase Shifter*

A steerable phased array antenna is designed operating at C/X-band [28] and at S-band [29]. The tunable phase shifter, implementing inkjet-printed barium strontium titanate (BST) thick-films, has a loaded-line topology as shown in Figure 3.5 & 3.6, where each unit cell consists of one varactor and inductance lines. The phase of the signal is varied by tuning the capacitance, which is implemented using the metal-insulator-metal (MIM) topology based on inkjet printing technology. Achieving a 46%

tunability at 8 GHz by applying 50 V across a 1.2 $\mu$m-thick BST film, the phase shifter is characterized by a figure of merit above 40°/dB from 7 to 8.5 GHz [28].

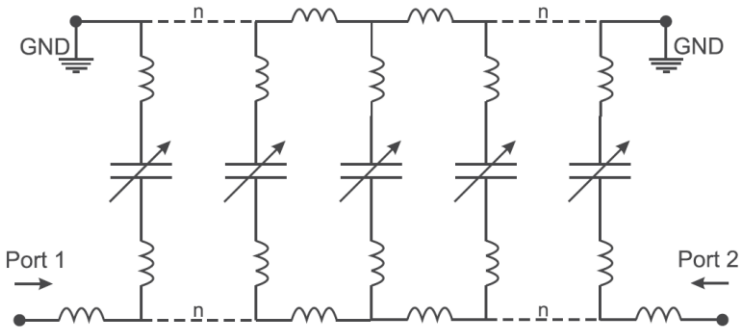


**Figure 3.5: Equivalent circuit of the loaded-line phase shifter [28].**

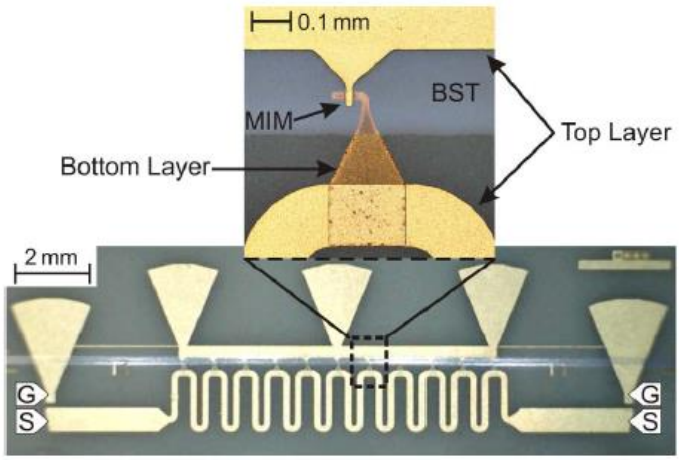


**Figure 3.6: Layout of the loaded-line phase shifter [28].**

As presented in [30], the phase shifter is designed based on the concept of the composite right/left-handed transmission line, and utilizes interdigital capacitor varactors (IDC) with inkjet-printed BST composite thick films as shown in Figure 3.7. The phase shifter occupies a total area of $0.16\lambda \times 0.24\lambda$ at 12 GHz, which is suitable for implementation in 2-D arrays. It achieves a 350° phase-shift at 12 GHz by applying a

biasing voltage of 180 V with a maximum insertion loss of 10 dB, resulting in a figure of merit of 35°/dB.

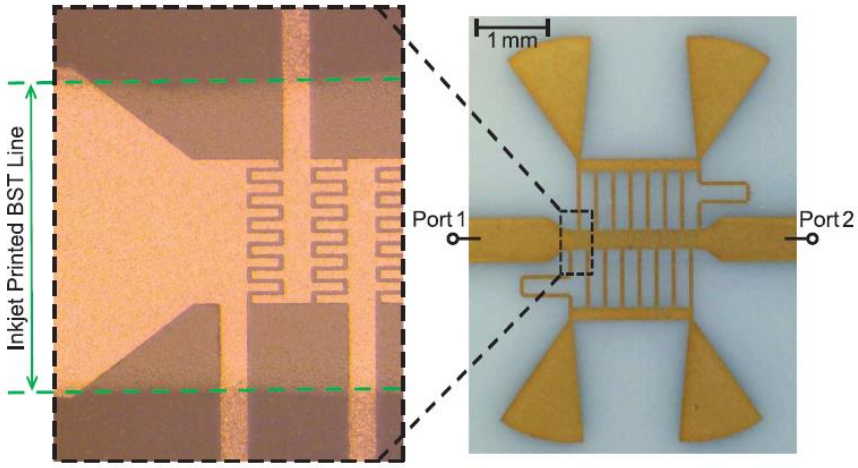


**Figure 3.7: Layout of the left-handed transmission line phase shifter [30].**

### *3.4.2 Reflective-Type Phase Shifter*

A compact and wide-band RTPS in 90 nm CMOS technology operating in V-band frequency range is presented in [31] as shown in Figure 3.8. It provides a 90° continuous phase shift over the frequency range of 50-65 GHz. Varactors in the reflective loads are implemented using CMOS transistors in which the source and drain terminals are connected together. By applying a variable voltage between the gate and drain/source of the MOS transistors, the capacitance value is varied. A broadside broadband coupler is employed as shown below.

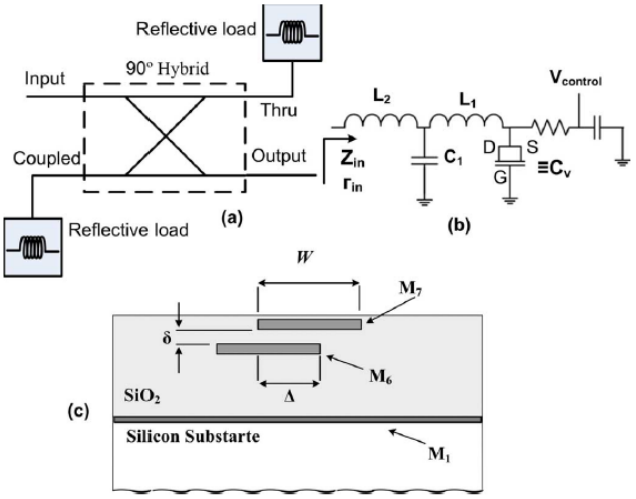


**Figure 3.8: RTPS block diagram with corresponding reflective load and the cross section of the broadside coupler [31].**

A compact 3-bit 90° RTPS is presented in [32] for phased-array applications at the 60 GHz ISM band (IEEE 802.11ad standard). As shown in Figure 3.9 & 3.10, a transformer-type directional coupler is used and shows a 50% size reduction compared to the broadside coupler presented in [31, 32]. The reflective loads are composed of binary-weighted digitally-controlled varactor arrays instead of analog tuning voltages compared to the conventional RTPS. The fabricated phase shifter in 65 nm CMOS technology, with its eight output states, exhibit a phase resolution of 11.25° with an RMS phase error of 5.2° and an insertion loss of 5.69 $\pm$ 1.22 dB at 60 GHz. This work presents the smallest circuit size (0.034 $mm^2$) and insertion loss among 90° phase shifters.

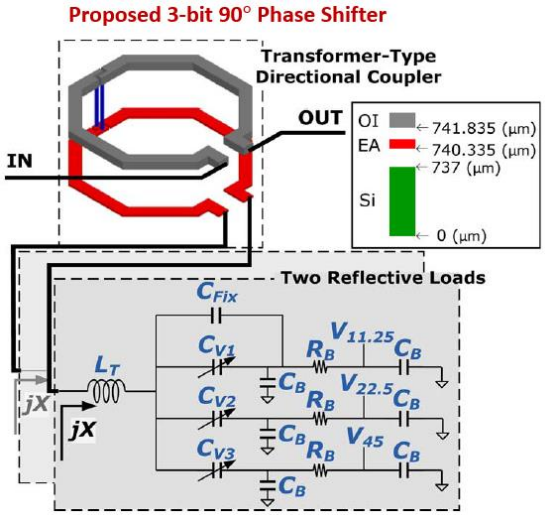


**Figure 3.9: 3-bit 90° RTPS [32].**

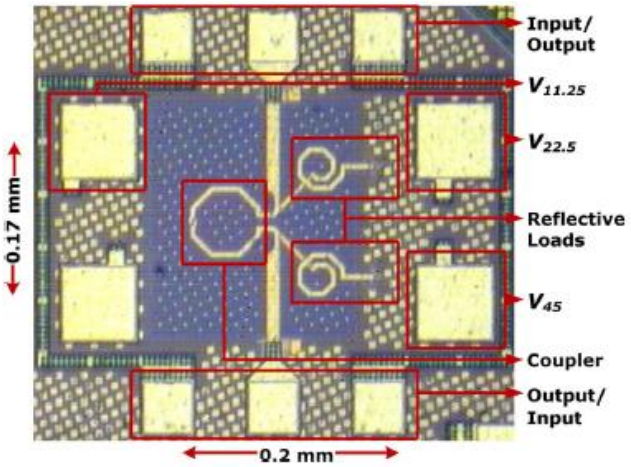


**Figure 3.10: Micrograph of chip die [32].**

A 24 GHz reflective-type phase shifter implemented in 0.18 μm CMOS technology is presented in [33] for phased array transmitters. Three stages of RTPS circuits employ hybrid couplers and capacitive-type reflective loads. They are cascaded in order to obtain a maximal phase-shift range of 185° with no DC power consumption. Note that the reflective loads employ AMOS varactors, with a tuning range of 3 and a phase span of about 69°, which are made by placing the n+ diffusion regions of an NMOS device in an N-well region. A continuously controlled switched π-attenuator is

used in front of the RTPS to provide a suitable gain control as shown in Figure 3.11 & 3.12. A constant insertion loss in all beam directions is mainly required for high-precision phased array systems, and the work presented in [33] achieves this requirement across the entire phase control range as shown in Figure 3.13.

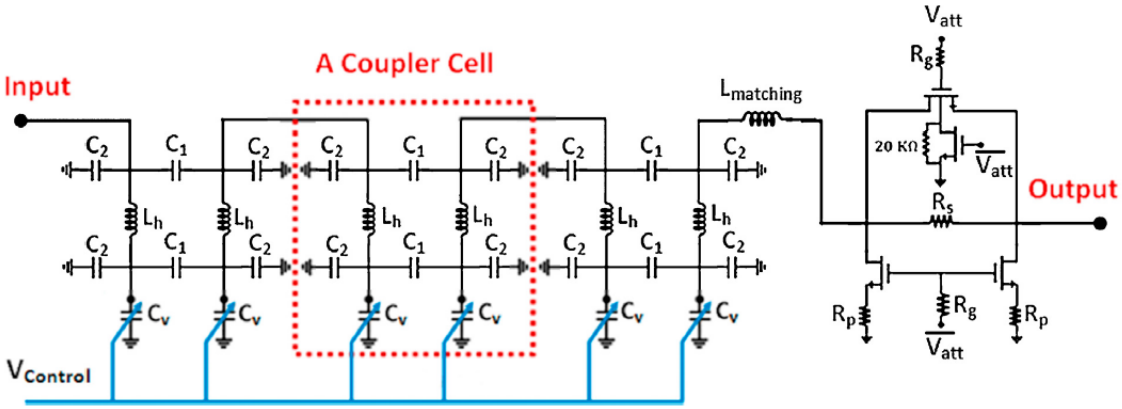


**Figure 3.11: Three RTPS cascaded stages with the switched π-attenuator [33].**

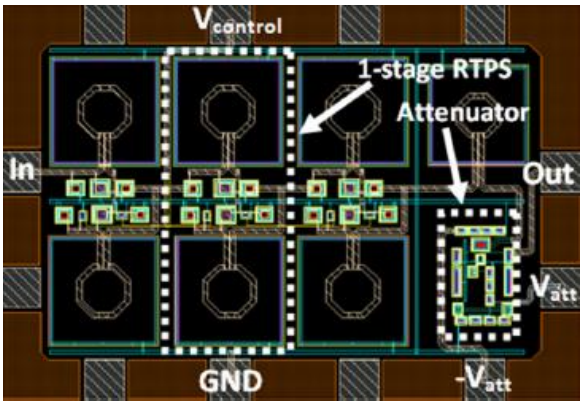


**Figure 3.12: Layout of the phase shifter [33].**

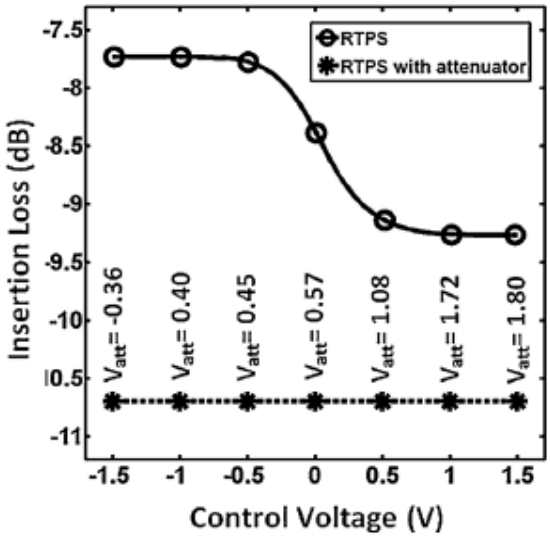


**Figure 3.13: Insertion loss vs. control voltage for RTPS with and without attenuator [33] .**

A 360° RTPS implemented in 100 nm InGaAs pHEMT technology is presented in [34]. By using a triple-resonating load technique as shown in Figure 3.14 & 3.15, a full 360° phase-shift range is achieved while minimizing the insertion loss variation to 9 $\pm$ 0.9 dB at 94 GHz. Note that the varactor in the triple-resonating mode is implemented using the 40 µm diode (i.e. number of fingers = 2, finger width = 20 µm) for the sake of balancing between the quality factor and the capacitance control ratio $\frac{C_{max}}{C_{min}}$. The inductors are realized as T-lines to resonate with $C_{max}$ and $C_{min}$.

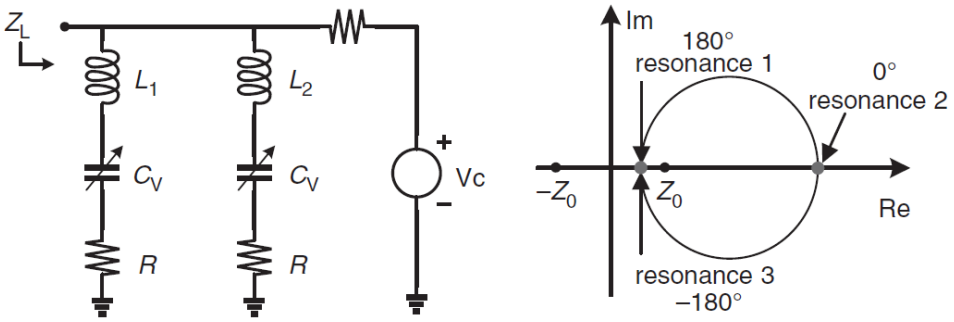


**Figure 3.14: Triple-resonating load schematic and its impedance in complex plane [34].**

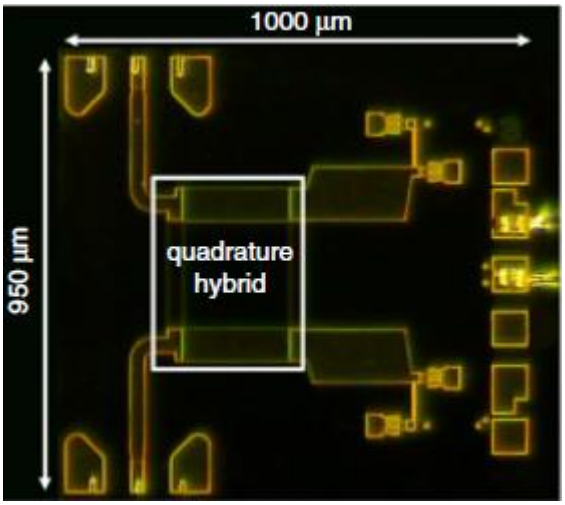


**Figure 3.15: Micrograph of the RTPS [34].**

### *3.4.3 RTPS with Switching Network*

An RTPS with single-stage commercially available varactor diodes at the reflective loads is presented in [35] to operate at 2.4 GHz ISM band for steerable antenna applications. Dual-branch switching network, cascaded to the output of the phase shifter as shown in Figure 3.16, is used to gain an additional 180° phase shift and to achieve a 360° phase shift range with limited capacitance range. A quarter-wavelength transmission line branch and a phase inverter branch constitute the switching network, where a single branch is selected and directed to the output port one at a time. Insertion loss variation is shown to be less than $\pm$ 0.5 dB across 1V to 9V bias voltages.

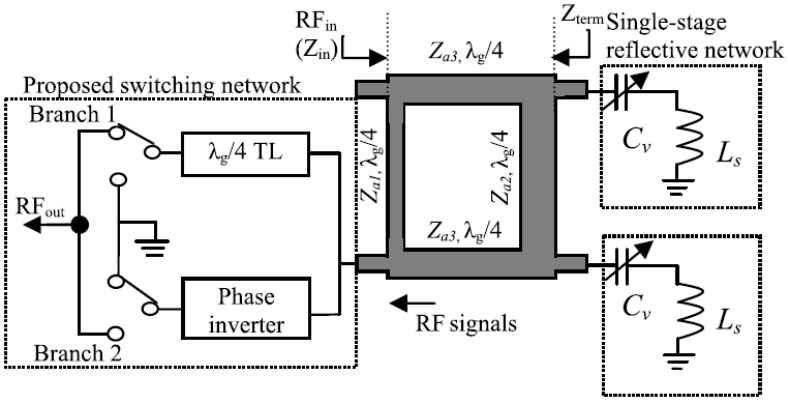


**Figure 3.16: Circuit diagram of the phase shifter with dual-branch switching network [35].**

## 3.5 Discussion

In this chapter, design requirements and common topologies of phase shifters are discussed. State of the art phase shifters are also presented. A reflective-type phase shifter surpasses its passive counterparts in terms of linearity, DC power consumption and simple control circuitry. Its main drawback is the high insertion loss added to the feeding network chain.

# CHAPTER 4

# RFIC IN CMOS TECHNOLOGY

## 4.1 Introduction

With the advent of new technologies, there exist several processes that are dedicated to RFIC design, starting from the low-cost ubiquitous silicon-based SiGe and CMOS technologies to advanced III-V material-based technologies. Chips based on III-V compound materials, however, such as GaAs and InP, suffer from low yield and high cost despite their low noise performance. On the other hand, favored for cost-sensitive consumer applications, CMOS and SiGe technologies [18, 36] present higher yield and improvement in the high frequency capacity in terms of their high unity-gain frequency $f_t$ [37] (in excess of 60 GHz and 200 GHz respectively) and maximum frequency of operation $f_{max}$. CMOS [38-40] surpasses SiGe technology in the fact that it presents the lowest cost choice in mass production. This low cost feature paves the way to a fully integrated mm-wave phased array system that encompasses both RF circuits, both analog and digital, and antennas on a single chip [23]. In this chapter, we focus on MOS varactors as key components in the reflective load of the RTPS, and three types are reviewed.

## 4.2 MOS Varactors

In general, MOS varactors are devices that behave like variable capacitors which are voltage dependent and steerable between $C_{min}$ and $C_{max}$. They are heavily employed as frequency tuning elements in the LC-tank VCOs. They can be also employed as the reflective loads in a RTPS.

Reverse biased p-n junction varactors comprise one option for realizing the variable capacitance. However, they present some limitations in terms of their non-scalability with technology as well as their low capacitance control ratio $\frac{C_{max}}{C_{min}}$, which limits the available frequency tuning range in LC-tank VCO and the RTPS phase-control range. They may also become forward-biased with large-amplitude swings, leading to additional losses in the circuits.

MOS transistors, commonly available in CMOS technology, portray themselves as a popular device to realize varactors. MOS-based varactors offer several advantages in terms of scalability and improved performance with every new process generation, as well as suitability for low power applications. Compared to p-n junction varactors, MOS varactors show higher capacitance versus area ratio leading to a wider tuning range and a high quality factor [41]. Higher doping levels in silicon lead to this improvement, and hence result in lower resistive losses, lower phase noise and lower power consumption [42].

The tuning capacitive range of a given varactor is given by the following equation:

$$\text{Tuning range} = \pm\frac{1}{2}\frac{C_{max}-C_{min}}{\frac{C_{max}+C_{min}}{2}} \tag{4.1}$$

where $C_{max}$ and $C_{min}$ are the maximum and minimum capacitance achieved in correspondence to the applied tuning voltage.

Technology scaling often leads to voltage supply reduction, thus realizing highly tunable varactors becomes a challenge due to the insufficient voltage headroom [43]. Voltage scaling has ceased a bit below 65nm due to device leakage considerations. The performance characteristics of a given varactor are given in terms of the power consumption, the tuning range and the phase noise contribution. There exist three main topologies for MOS varactors: the traditional D=S=B structure, the IMOS structure and the AMOS structure.

### *4.2.1 D=S=B Varactor*

The traditional D=S=B structure is realized by connecting the drain, the source and the bulk together. The capacitance is varied by controlling the voltage $V_{BG}$ between the bulk (B) and the gate (G). In this topology, the varactor exhibits three operating regions as shown in Figure 4.1: inversion, accumulation and depletion region. Its small-signal C-V characteristic presents a non-monotonic function of the biasing voltage $V_{BG}$. In both the inversion and accumulation regions, the gate-oxide capacitance is given by:

$$C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} = C_{max} \tag{4.2}$$

where A = $Width \times Length$ is the transistor channel area, $t_{ox}$ the oxide thickness and $\varepsilon_{ox}$ the permittivity of the silicon dioxide.

A series capacitor $C_{dep}$ is added to the gate-oxide capacitance in the depletion region which is approximately equivalent to $C_{min}$, when the depth of the depletion layer reaches its maximum.

### *4.2.2 IMOS Varactor*

Decoupling the bulk of the D=S=B varactor from both the source and the drain, and tying it to the ground (NMOS) or to the highest available DC-voltage $V_{DD}$ (PMOS), results in an IMOS varactor which exhibits a wider tuning capacitance range compared to the D=S=B structure [44]. The IMOS varactor is prohibited from entering the accumulation region for a very wide range of gate voltage. As shown in Figure 4.2, the C-V characteristics display a monotonic function of the tuning voltage $V_{GS}$.

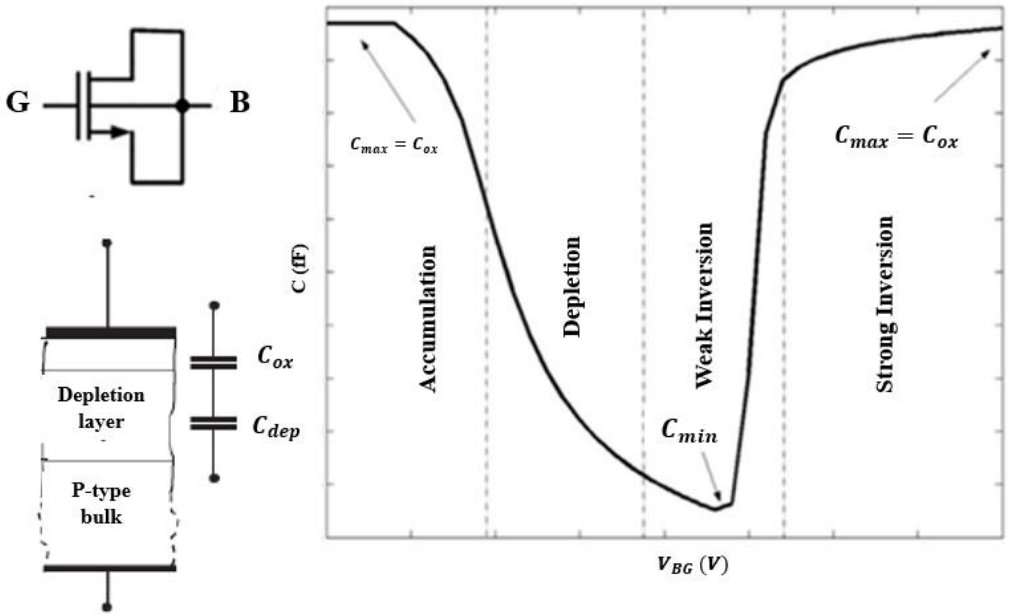


**Figure 4.1: C-V Tuning Characteristics of an NMOS transistor with traditional D=S=B structure [45].**

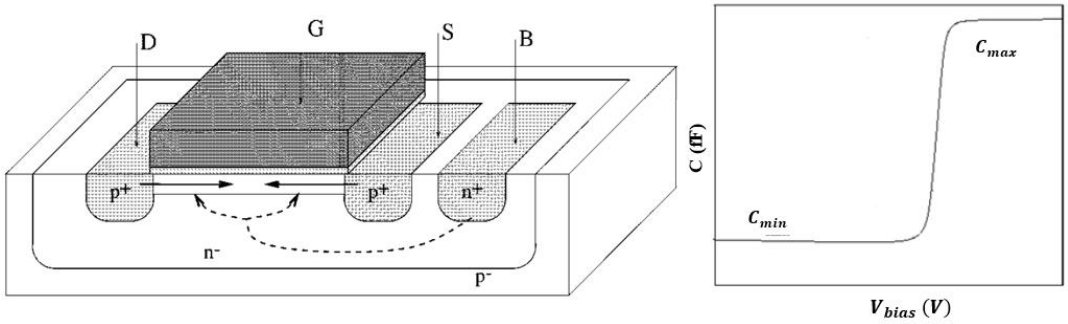


**Figure 4.2: IMOS varactor and its C-V characteristic [44].**

### *4.2.3 AMOS Varactor*

As shown in Figure 4.3, the AMOS varactor structure [46] is derived from a PMOS transistor in an n-well, where the p+ doped source/drain regions are replaced by n+ well contacts, thereby prohibiting the varactor from entering the inversion region (weak, moderate and strong) due to the suppression of holes injected into the MOS channel. Operating only in the accumulation and depletion regions, the AMOS C-V characteristic is also non-linear and monotonic resulting in a wider tuning capacitance range compared to the D=S=B varactor [44].

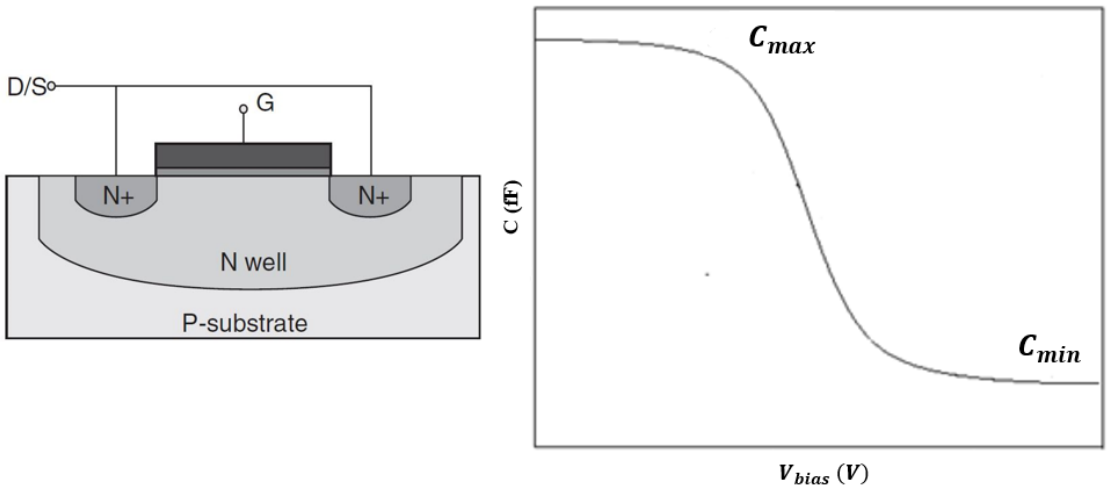


**Figure 4.3: AMOS varactor and its C-V characteristic [47].**

### *4.2.4 Other Configurations*

Several methods are employed in the literature in order to widen the varactor tuning range. For instance, a resistors-added IMOS varactor is used in [48] where large resistors are connected to the source and the bulk. This lowers the minimum capacitance in the depletion mode, cancels the MOSFET parasitic capacitances, and it maintains the maximum capacitance in the inversion mode. It also expands the capacitance tuning range to $\pm 46.1\%$ which is $\pm 15.6\%$ higher than a conventional MOSFET varactor, and allows a wide tuning for a millimetre-wave VCO using 0.18 $\mu m$ standard CMOS process. It is also shown [49, 50] that connecting the gate to the source through an external capacitor supplements additional capacitance in the inversion mode, hence increasing the varactor's maximum capacitance and the tuning range up to $\pm 66\%$ in a 90 nm industrial CMOS process.

## 4.3 Discussion

CMOS technology is heavily used in the implementation of phase shifters due to its low cost and high-performance characteristics. Such features allow the full integration of mm-wave phased arrays on a single chip. MOS-based varactors are typically favored for use in reflective loads, which are in their turn used to terminate both the coupled and through ports of the hybrid coupler. A detailed presentation of the different types of MOS-based varactors is shown. The AMOS-based varactor is shown to surpass its counterparts, i.e. the IMOS and the traditional D=B=S varactors, in terms of its high phase shift range.

# CHAPTER 5

# SOFTWARE CONTROL OF BACK END CIRCUITRY

## 5.1 Introduction

A software algorithm is developed in order to extract the scattering parameters, or S-parameters, from the back end circuitry, such as measurement devices or antenna arrays components, similar to the functionality of a vector network analyzer (VNA) [51, 52]. This is done by processing the magnitude and phase of the incident and reflected waves from the network using Arduino open-source platform.

## 5.2 Operation

As shown in Figure 5.1 & 5.2, the mode of operation of the network is as follows:

- The RF source is set to sweep over a specified bandwidth.
- The generated signal is coupled with a dual directional coupler that couples the travelling wave in one direction into one of its ports.
- Both the reflected and incident waves are down-converted to 1 MHz intermediate frequency (IF) using a mixer in each path.
- The filtered 1 MHz signals are down-converted to 1 kHz signals by the aid of AD633 analog multiplier since the maximum reading rate of the internal ADC of the Arduino is 10 kHz.

- The filtered 1 kHz signals are then inputted in the Arduino Mega 2560 board for processing, which has 256 KB of flash memory for storing code, 8 KB of SRAM and 4 KB of EEPROM.

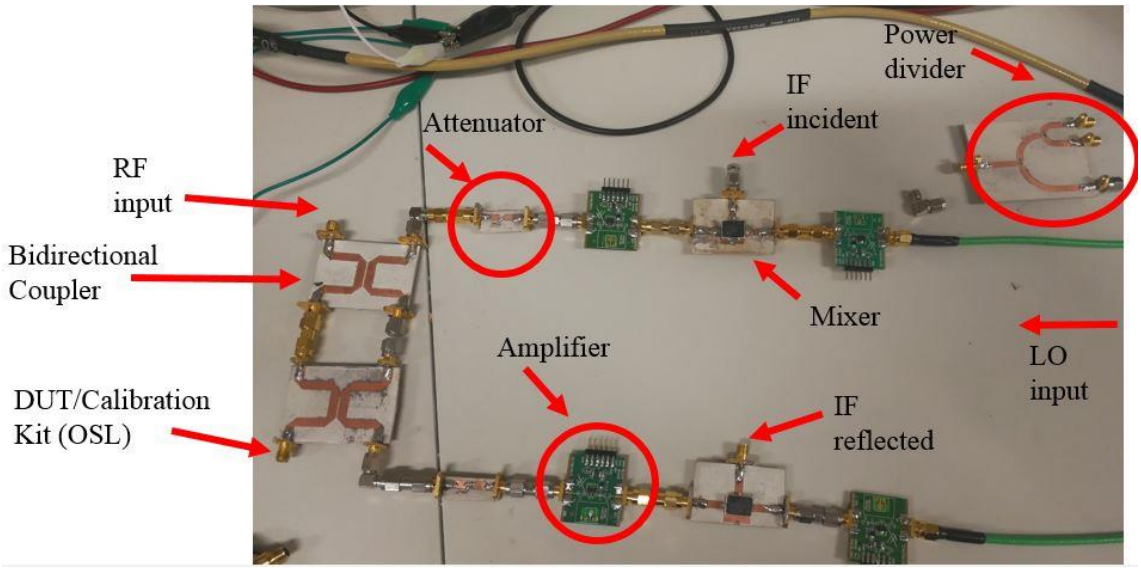


**Figure 5.1: Vector Network Analyzer.**

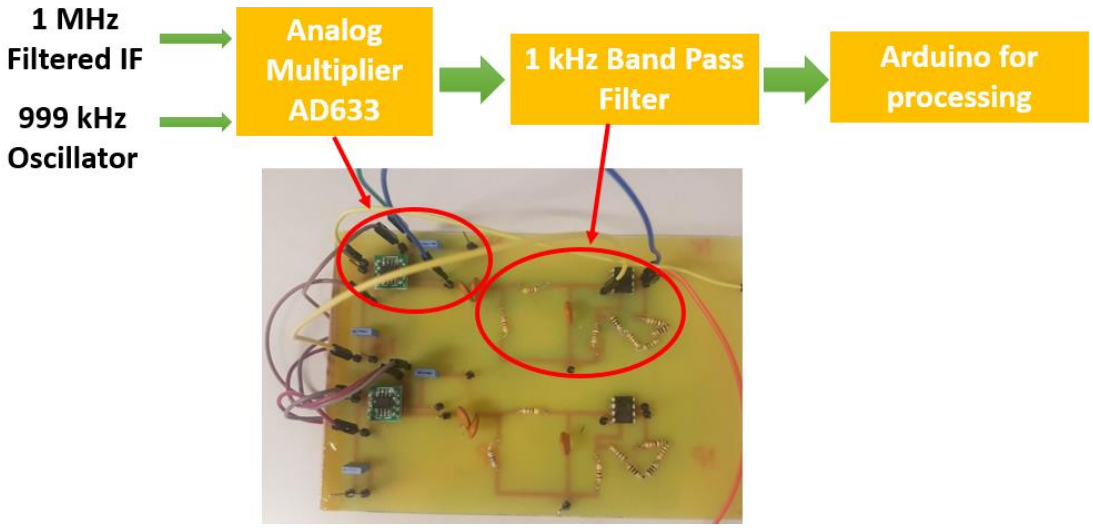


**Figure 5.2: Down-conversion circuit from 1 MHz to 1 kHz for Arduino processing.**

## 5.3 Data Acquisition and Processing

Figure 5.3 shows the block diagram of the different stages of the data acquisition and processing in Arduino including the compensation parameters extraction as well as the S-parameters extraction of a given device under test (DUT).

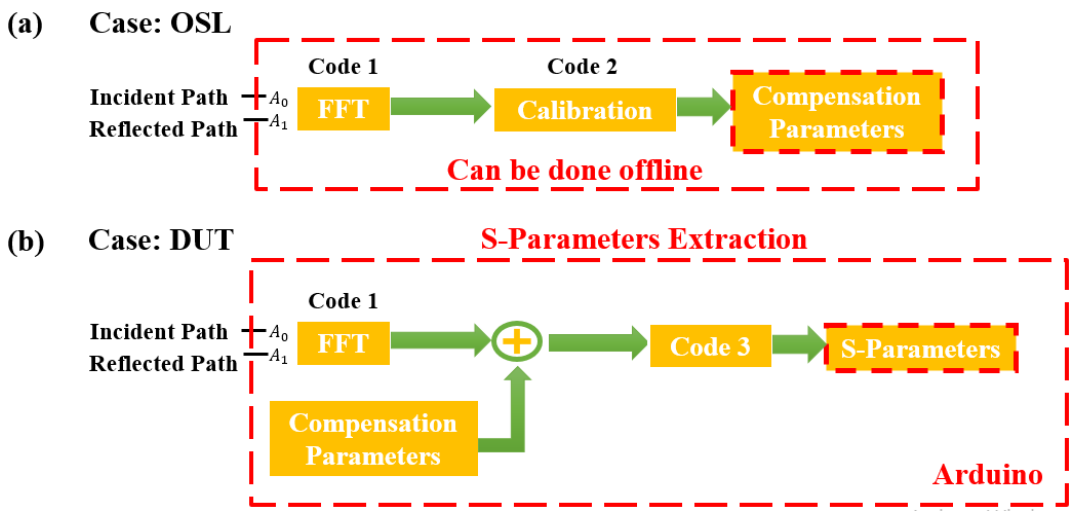


**Figure 5.3: Block diagram summarizing the different stages for (a) Compensation parameters extraction (b) S-Parameters extraction.**

### *5.3.1 Fast Fourier Transform (FFT) Stage – Code 1*

The FFT stage includes the following steps to get the raw S-parameters data:

- The time-domain signal for both the incident and the reflected paths are inputs to the Arduino through two analog pins.
- The FFT algorithm is performed by sampling the signal over a period of time and dividing it into its frequency components, outputting both the magnitude and the phase of the corresponding 1 kHz signal. This is accomplished using the FFT library inside Arduino.

### *5.3.2 Arduino's Challenges – FFT Signal Processing*

The two paths are not read simultaneously by Arduino. Using the wall clock time (the sum of the CPU time, I/O time, and the communication channel delay), the time delay between them is accounted. However, it is shown by relying on MATLAB [53] that Arduino is not sampling at the exact time step, but rather sampling slightly slower than the defined sampling frequency and each time at a different rate due to implicit uncertainty, which is a challenge to be addressed. Such effect is illustrated in Figure 5.4, where for the same signal input to two analog pins on Arduino, the results do not superimpose after taking into account the time delay. A suggested solution is to use a microcontroller that is able to read two inputs simultaneously and sample them both at the same fixed sampling frequency.

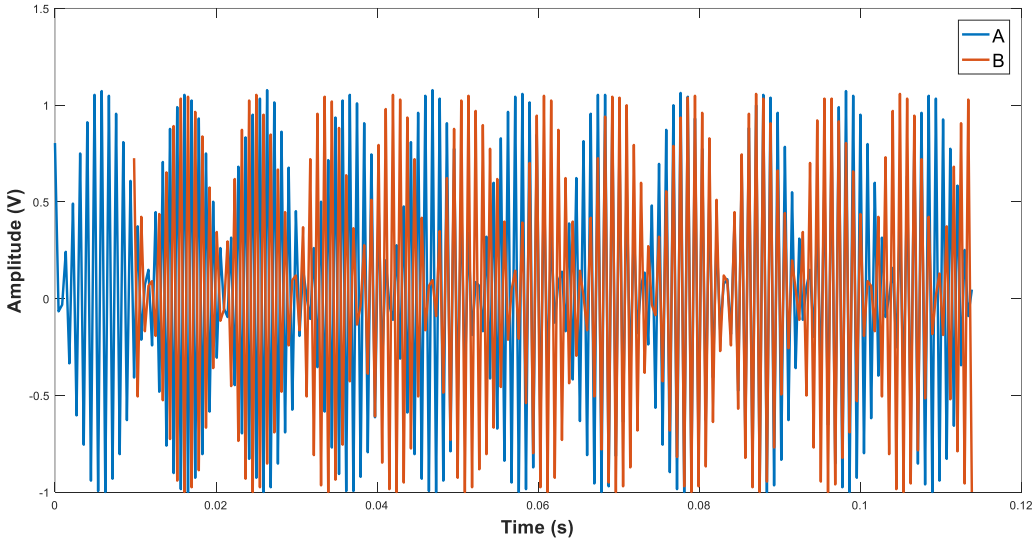


**Figure 5.4: Illustration of the non-fixed sampling frequency of the Arduino's ADC**

### *5.3.3 Overall Calibration Phase – Code 2*

A software calibration algorithm is implemented in the code in order to remove the repeatable measurement errors due to the imperfections in the measurement setup. Since the calibration will be the same for a given network, it can be done just once. In this phase, since the calculations involve complex numbers and matrices, two special standalone libraries are used (MatrixMath.h & Complex.h), and these are combined together in order to be able to perform the calculations.

As shown in Figure 5.3 (a), while performing the OSL calibration for three different loads (Open/Short/Load) using the calibration kit, the steps to extract the compensation parameters can be summarized as follows:

- Read the incident path, perform FFT, and the results are stored in a text file in the SD card.
- Repeat for the reflected path.
- Process these text files into the code inside Arduino or MATLAB to compute the compensation parameters in order to use them later on.

### *5.3.4 S-parameters Extraction – Code 3*

As shown in Figure 5.3 (b), once the compensation parameters are computed, measurement of DUT can be initiated, where the incident and the reflected waves of the DUT are processed by the Arduino. Taking into consideration the compensation parameters, the ratio of the reflected wave over the incident wave is computed in order to get the actual S-parameters data.

As a final output, the code written in Arduino is used to calculate and save the magnitude and the phase of the scattering parameters of the DUT for the desired frequency range (700 MHz-3 GHz) on a text file on the SD card module. Note that this work can be extended to any two-port network. For more details, we refer the reader to [51, 52].

## 5.4 Discussion

In this chapter, a software control of back end circuitry is discussed, and three main codes were written in C-language:

- Code 1 is intended to extract the response of the device under different conditions (open/short/load and DUT).
- Code 2 is intended to compute the compensation parameters extracted in the calibration phase.
- Code 3 is intended to compute the actual S-parameters by combining the raw data of the DUT and the compensation parameters.

Despite Arduino's challenges, this work achieved the implementation of a software algorithm intended to extract the S-parameters of antenna array's components, which is useful for the back end circuitry.

# CHAPTER 6

# A FOUR-ELEMENT LINEAR PHASED ARRAY AT MICROWAVE FREQUENCIES

## 6.1 Introduction

The main objective of this chapter is to validate the beam steering capability of the radiation pattern of a phased antenna array. A four-element linear phased array, which is inspired by the work in [11] and which was designed at 7.9 GHz, is redesigned to operate at 2.5 GHz. The array is fabricated and tested along with its feeding network.

## 6.2 $4 \times 1$ Four Series-fed Microstrip Antenna Array - Review

The work discussed in [11] is first reproduced by simulating a 4×1 linear array at 2.4 GHz as shown in Figure 6.1. Each of the linear array elements is based on four series-fed microstrip antennas built on a stack of two layers of the same 1.57-mm thick substrate Rogers RT/duroid 5880 ($\varepsilon_r$ = 2.2 &tan $\delta = 0.0009$). A ground plane separates the two layers.

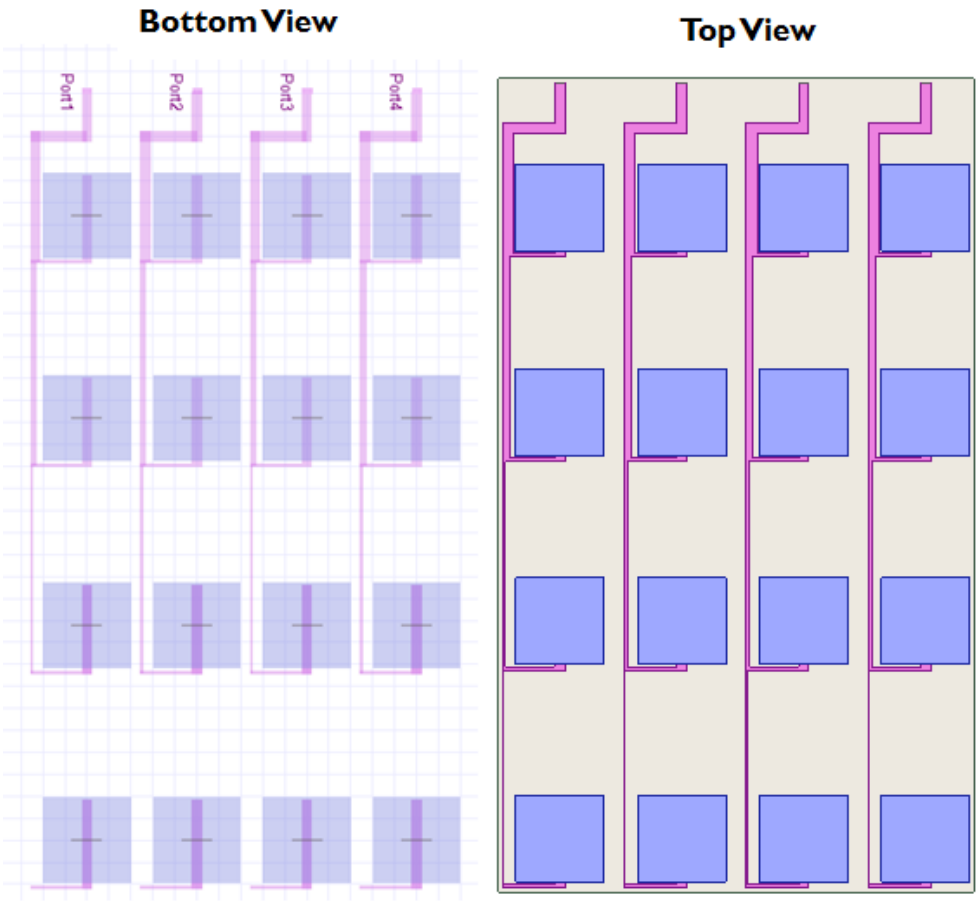


**Figure 6.1: 4×1 linear array with its elements based on four series-fed microstrip antennas.**

By optimizing the substrate electrical parameters, the feed line width, as well as the slot size and position, the aperture-fed patch antenna is designed at 2.4 GHz using the electromagnetic simulation software AED HFSS 18.2 [4]. The simulated antenna reflection coefficient for the series-fed array is shown in Figure 6.2.

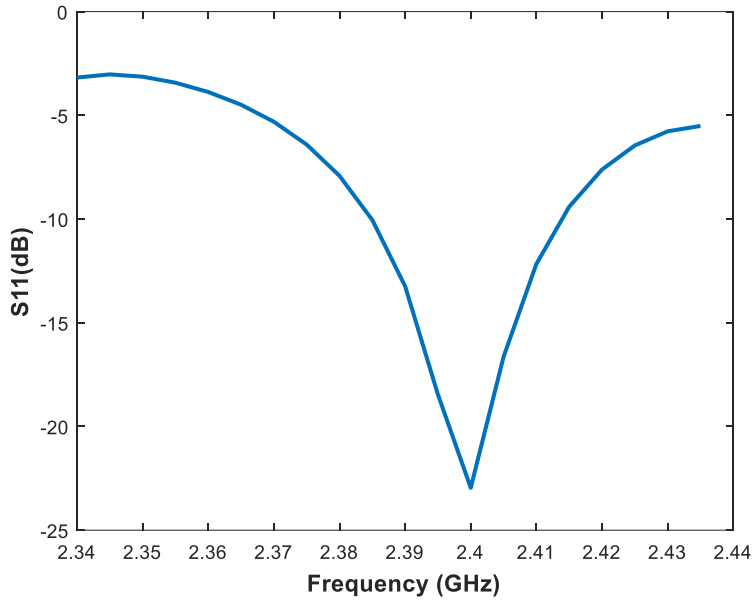


**Figure 6.2: Simulated Impedance match for the 4-element antenna.**

## 6.3 Our Fabricated 4 × 1 One Aperture-fed Patch Antenna Array

The four series-fed microstrip antennas is replaced by one aperture-fed microstrip antenna for a more compact design as shown in Figure 6.3. Note that the elements in the antenna array are spaced at $0.5\lambda$. The simulated and measured reflection coefficient for the aperture-fed patch antenna operating at 2.5 GHz are shown in Figure 6.4.

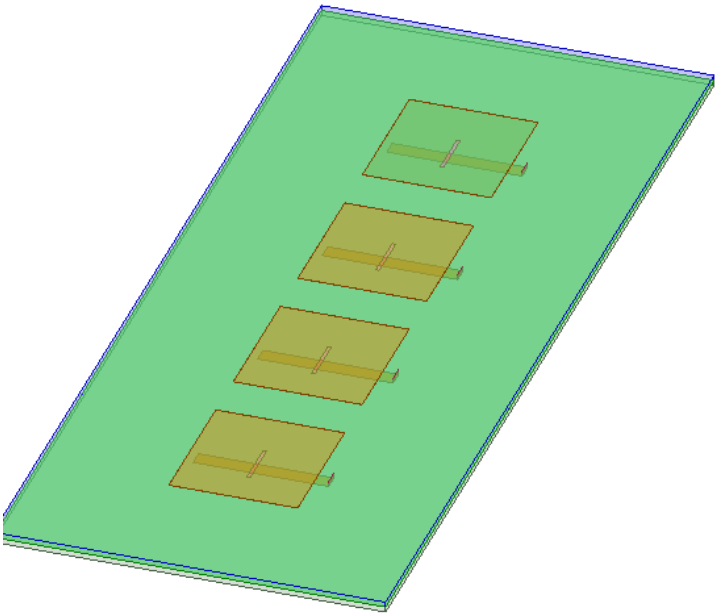

**Figure 6.3: 4×1 One Aperture-fed Patch Antenna Array.**

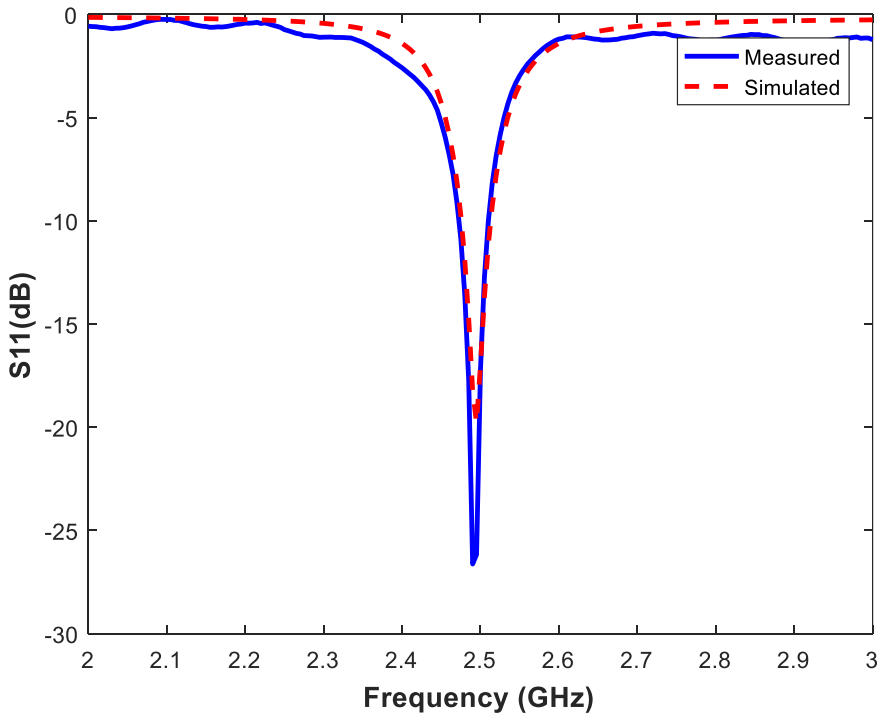


**Figure 6.4: Reflection coefficient for the one aperture-fed patch antenna operating at 2.5 GHz.**

The feeding network of the 4-element linear phased array, designed at microwave frequencies (2.5 GHz), consists of: three power dividers, two phase shifters, two attenuators, and a transmission line board, feeding a 4×1 aperture-fed patch antenna array. The fabricated prototype is shown in Figure 6.5.

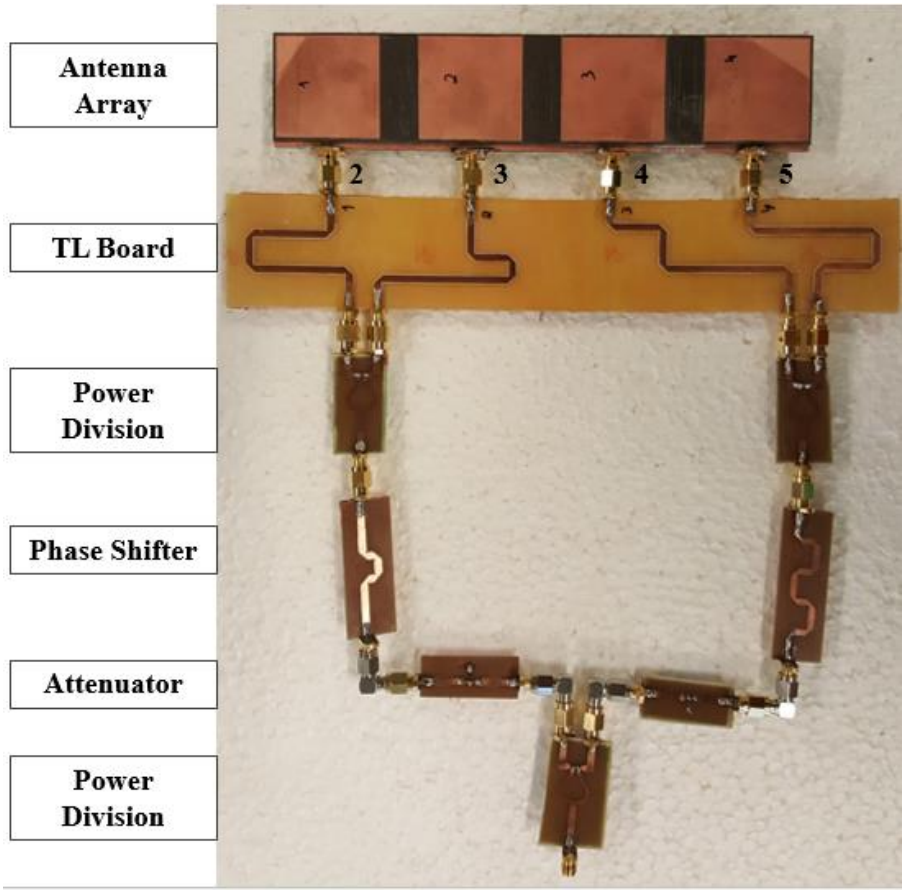


**Figure 6.5: Our fabricated 4×1 linear array with its feeding network.**

The input power is divided using a 1-to-2 Wilkinson equal power divider, so that its outputs have equal magnitude and equal phase. Then, for each output, a taper is applied using a 5 dB T-pad attenuator, followed by a PS implemented as transmission line of a given length (true-time delay units: $\theta = \beta l$, where the phase shift $\theta$ is controlled by the electrical length). The two PSs are made using different effective lengths of transmission

lines resulting in a 90° phase shift between ports 2/3 and 4/5 respectively. The output of each PS is connected to a 1-to-2 Wilkinson equal power divider. Each of the four outputs are connected to the 4×1 antenna array through a 4-to-4 transmission line board, which is used to conserve the phase from each of the four power divider outputs.

The PSs, the attenuators, the power dividers as well as the transmission line board are designed and constructed on a 1.6-mm-thick FR4 at 2.4 GHz using Advanced Design System (ADS) [54]. The phase shifts at the four outputs of the transmission line board are shown in Figure 6.6.

By importing the solution data from ADS to AED HFSS circuit, the antenna array with its feeding network is simulated. The simulated and measured reflection coefficient of the whole array is shown in Figure 6.7. Note that there is a good match at the frequency of interest, i.e. 2.5 GHz. The oscillations in the results are due to the need to re-calibrate the vector network analyzer used for measurements.

Radiation pattern measurements are performed in the anechoic chamber, where the transmit-receive system is composed of the 4×1 linear array with its feeding network as the transmitter and a horn antenna as the receiver separated by a distance of 4.3 m. The simulated and measured radiation pattern at 2.5 GHz are well-matched as shown in Figure 6.8, showing that the beam was steered to approximately 15°.

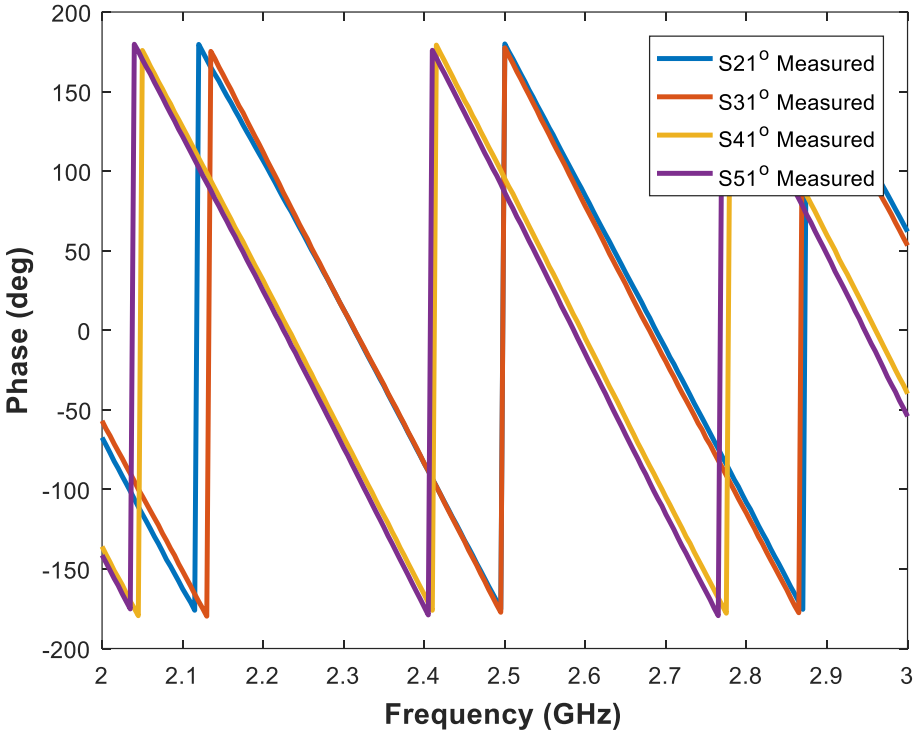


**Figure 6.6: Phase outputs at the four ports of the transmission line board.**

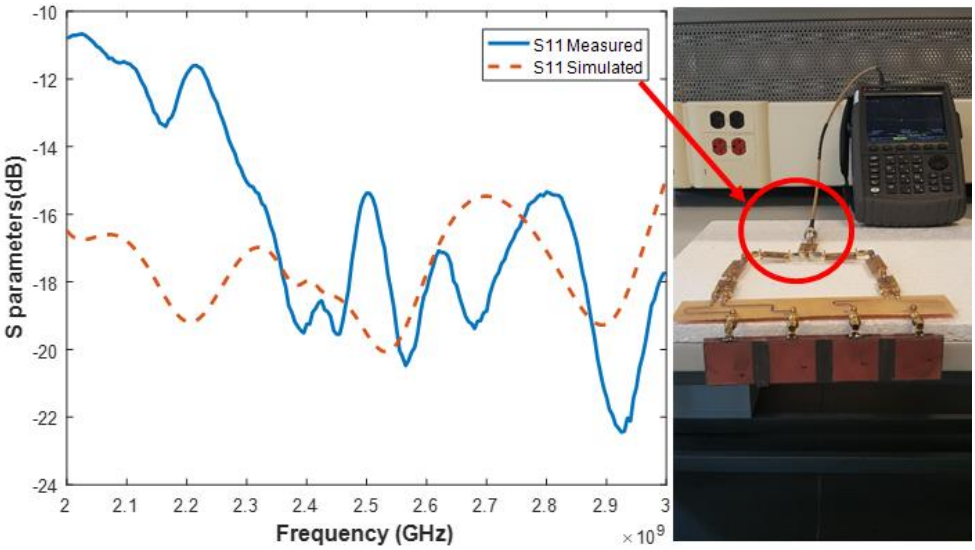


**Figure 6.7: Reflection coefficient of the array.**

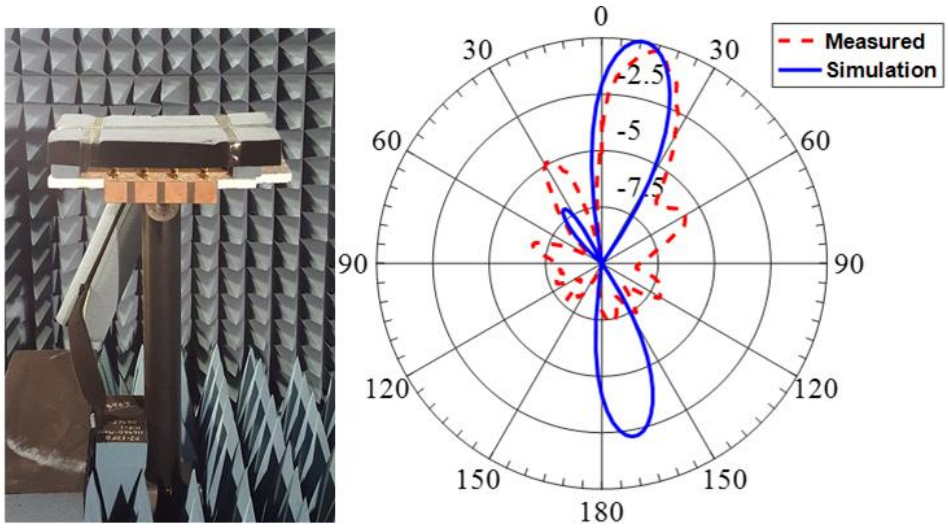


**Figure 6.8: Radiation Pattern at 2.495 GHz.**

## 6.4 Discussion

In this chapter, a 4×1 one aperture-fed patch antenna array with its feeding network is re-designed at microwave frequencies inspired by the work presented in [11]. The feeding network consists of three power dividers, two phase shifters and two attenuators. There is a good match for the full array at 2.5 GHz. The radiation pattern of the phased array is shown to be steered to approximately 15° validating its beam steering capability.

# CHAPTER 7

# MILLIMETER WAVE REFLECTIVE TYPE PHASE SHIFTER DESIGN

## 7.1 Introduction

In this chapter, the design of a new millimeter wave reflective type phase shifter is presented. The phase shifter is designed to operate at 60 GHz and it is implemented by employing 90 nm industrial CMOS process. First, section 7.2 describes the integrated circuit design flow. In section 7.3, a review of the RTPS is presented in terms of its constituent blocks. Sections 7.4 and 7.5 are dedicated to the 3-dB hybrid coupler and the proposed reflective load designs respectively. Finally, the overall phase shifter design is discussed and presented along with all of its key characteristics based on post-layout simulations in sections 7.6 and 7.7.

## 7.2 Integrated Circuit Design Flow

As shown in Figure 7.1, analog/RF IC design necessitates a solid background in different areas such as IC design, semiconductor processes, CAD tools, transceiver architectures, and others. In fact, there is no single simulation tool that can handle such IC design since EM simulation is needed using either AED HFSS or ADS Momentum, as well as circuit simulation and final layout are done via Cadence Virtuoso [3]. Note that EM support has been recently introduced in the Cadence tool suite, but such capabilities were not available at our disposal during the execution of this thesis.

Figure 7.2 shows the RFIC design flow starting from defining the system specifications and ending up with the chip fabrication and measurement. Across this flow and after the layout creation, we focus on three main steps that need to be met prior to post-layout design characterization:

- Design Rule Checking (DRC): checks whether any dimensions violate the design rule of the technology.
- Layout versus Schematic (LVS): determines whether any discrepancy exists between the schematic and the layout.
- Parasitic Extraction using Xcalibre (PEX): used to extract the parasitic elements from the layout.

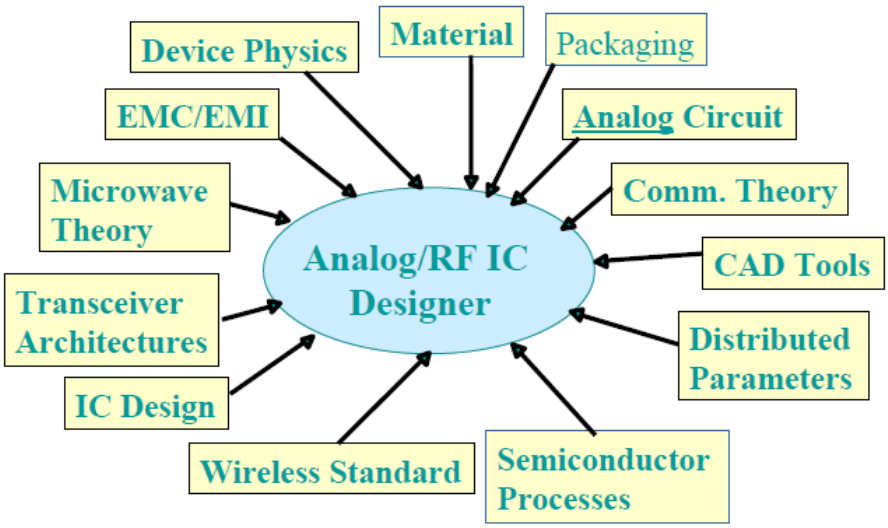


**Figure 7.1: Analog/RF IC Designer Expertise.**

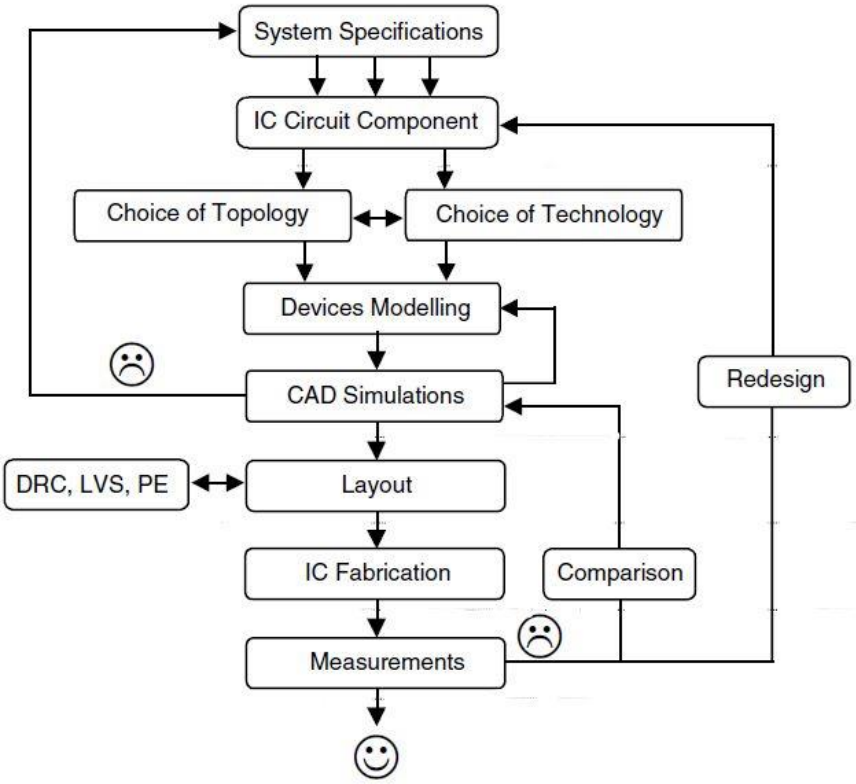


**Figure 7.2: RFIC Design Flowchart [55].**

## 7.3 RTPS Review

As introduced in previous sections, an RTPS consists of a 3-dB 90° hybrid coupler terminated with two identical reflective loads at the through and the coupled ports. The hybrid or quadrature coupler equally divides the input signal into two signals 90º out of phase, then these signals reflect from the pair of reflective loads, cancel out at the input port (out-of-phase), and combine in phase at the phase shifter output (the isolated port) as shown in Figure 7.3. For our designs, the hybrid coupler was implemented in ADE HFSS 3D layout using 90nm industrial technology layer characteristics. The reflective load was designed and simulated using Cadence virtuoso layout editor also using 90nm industrial technology.

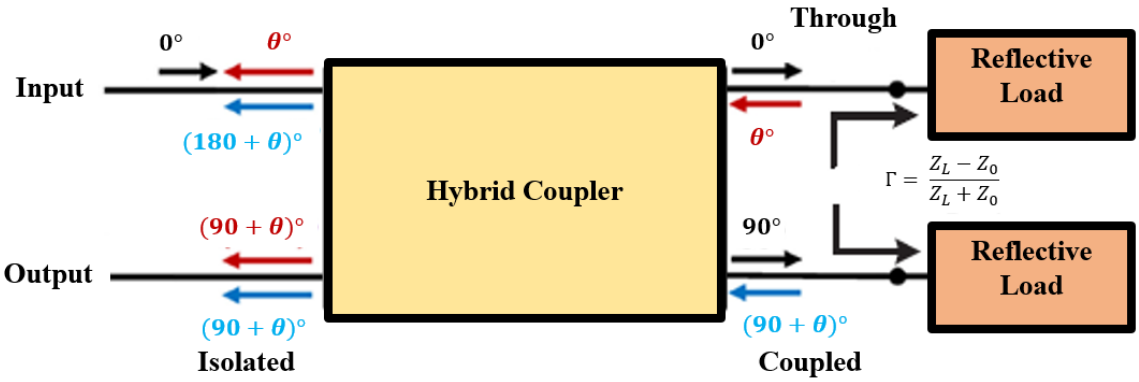


**Figure 7.3: Reflective Type Phase Shifter Topology.**

## 7.4 3-dB Hybrid Coupler

In this section, the design of a 3-dB quadrature hybrid coupler at 60 GHz is presented in details in terms of its operation, its different implementations, the design and the EM simulation results using AED HFSS 3D Layout.

### *7.4.1 Overview*

#### 7.4.1.1 Operation

Hybrid couplers are passive devices widely used in microwave and millimeter-wave applications in order to provide equal power division with constant phase difference within the operating frequency band. They are widely employed in mixers, modulators, power amplifiers, and antenna beam forming networks, mainly Butler matrices and reflective-type phase shifters.

Hybrid couplers are usually 3 dB directional couplers with four ports, with a defined 90° phase difference in the outputs of the through and coupled arms. With all ports matched, power entering port 1 is evenly divided between ports 2 and 3, with a 90° phase shift between these outputs. No power is coupled to the isolated port 4. Note

that the quadrature hybrid has a high degree of symmetry, so that any port can be used as the input port.

#### 7.4.1.2 Different Implementations

The quadrature hybrid, also known as the branch-line coupler, is commonly implemented using either the distributed model or the lumped model depending on the frequency of operation and the intended application.

##### 7.4.1.2.1 Distributed Model

The hybrid coupler can be implemented using the distributed model by relying on microstrip T-lines as shown in Figure 7.4. This type of implementation is suitable at millimeter wave frequencies, for frequencies higher than 30 GHz. It is characterized by a narrow-band response since the wavelength $\lambda$ is frequency dependent. It will be adopted to design our phase shifter since our application is at 60 GHz and does not need a wide-band characteristic.

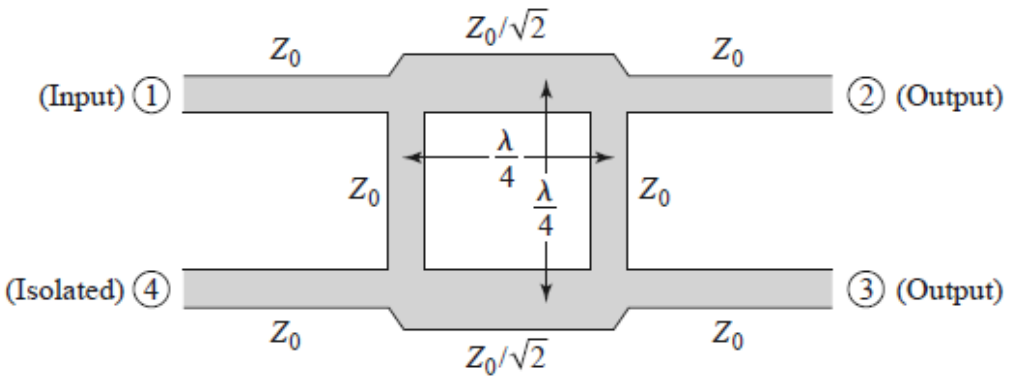


**Figure 7.4: Geometry of a branch-line coupler [56].**

7.4.1.2.2 Lumped Model

The distributed model is not suitable for frequencies below 30 GHz since microstrip lines become bulky and consume a large area. Therefore, at these frequencies, the hybrid coupler is implemented using the lumped model, i.e. distributed elements, to achieve low form factor as shown in Figure 7.5. This is not the case of our design.

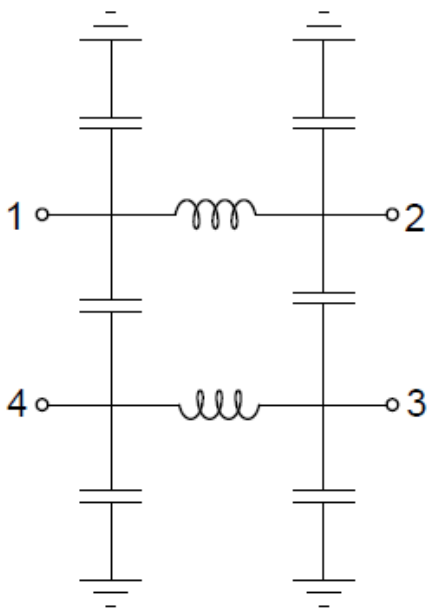


**Figure 7.5: Lumped implementation of the hybrid coupler.**

### *7.4.2 Implementation and Results*

We implemented a distributed 3-dB hybrid coupler shown in Figure 7.1 using AED HFSS 3D Layout. The characteristics (thickness, dielectric constant) of the substrate, the ILD (Inter-Layer Dielectric), the IMDs (Inter-Metal Dielectrics) as well as the metal stack of the 90 nm industrial technology, are retrieved from the design manual, and inserted into AED HFSS. A cross-section view through the metal stack of

the CMOS VLSI technology is shown in Figure 7.6, presenting both the BEOL (Back End Of Line) and the FEOL (Front End Of Line).

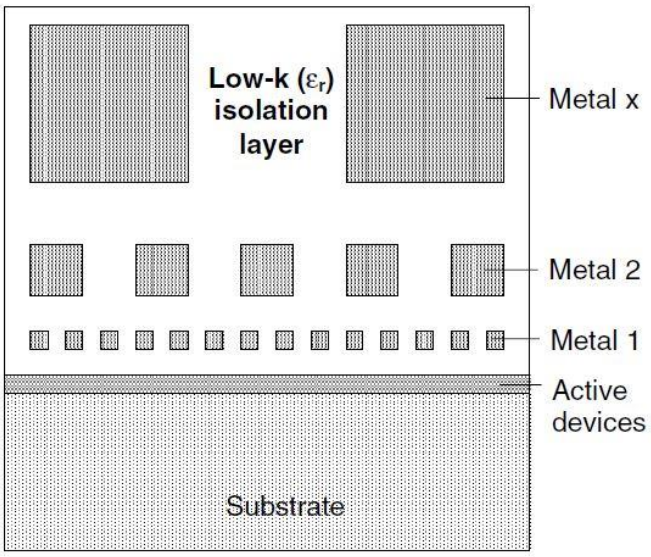


**Figure 7.6: Cross-section view through metal stack of CMOS VLSI technology [55].**

The thickness of the metals increases towards the top of the wafer, while the sheet resistance decreases. For this reason, the ultra-thick metal (UTM) M9 is chosen to carry the RF signal, while the bottom layer M1 is chosen as the ground plane. Note that the loss tangent of all the dielectric layers is assumed to be 0.01 for simulation purposes. The 700 $\mu m$-thick silicon substrate is characterized by high conductivity (10 S/m) and a high dielectric constant ($\varepsilon_r = 11.9$).

The conductivity $\sigma$ of each metal layer is given by the following formula [57]:

$$\rho = R_s * t$$

$$\sigma = \frac{1}{\rho}$$

$\rho$ is the metal resistivity ($\Omega.\mu$m), $R_s$ the sheet metal resistance ($\Omega$/sq) and t is the metal thickness ($\mu$m). These parameters are retrieved from the technology file.

Simulations have shown that the characteristic impedance of the transmission line ranges from 70 Ω up to 100 Ω based on the dimensional constraints enforced in the design rule manual of the 90 nm industrial node. Therefore, we chose $Z_0$ = 100 Ω to be our reference impedance. Note that design rules enforce minimum and maximum allowable widths for the different metal layers (M1 up to M9). They also enforce minimum spacing between two metal lines, and specify the required metal densities.

Figure 7.7 shows the initial design of the hybrid coupler in AED HFSS 3D Layout, with a continuous ground plane, operating at 60 GHz, and occupying an area of 0.672 $mm^2$. As stated previously, in this design, M1 (in blue) is acting as the ground plane while M9 (in green) as the signal line.

Figure 7.8 shows the simulated S-parameters results in dB of the designed hybrid coupler with continuous ground plane, where the return loss (RL) is at least 25 dB at 60 GHz, presenting a perfect matching at each port. The magnitude of $S_{41}$ shows the isolation between port 1 and port 4 is higher than 25 dB at 60 GHz.

Figure 7.9 shows the quadrature phase difference in the outputs of the through and coupled arms of the hybrid coupler.

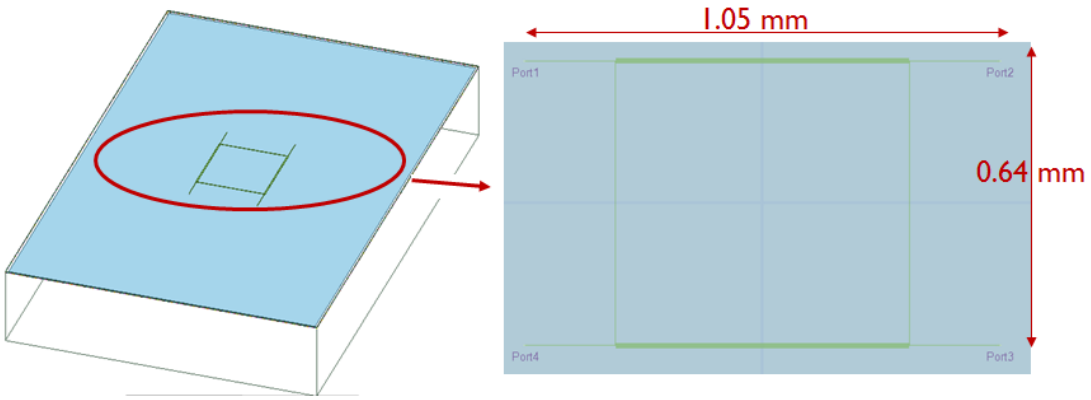


**Figure 7.7: Initial design of the 60 GHz hybrid coupler with a continuous ground plane.**

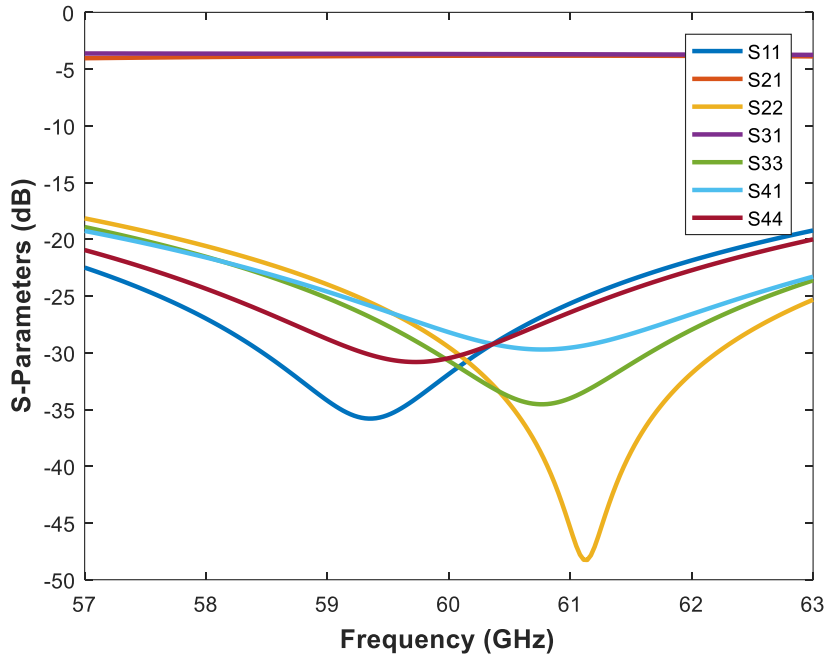


**Figure 7.8: Simulated S-parameters (dB) of the hybrid coupler in Figure 7.7.**

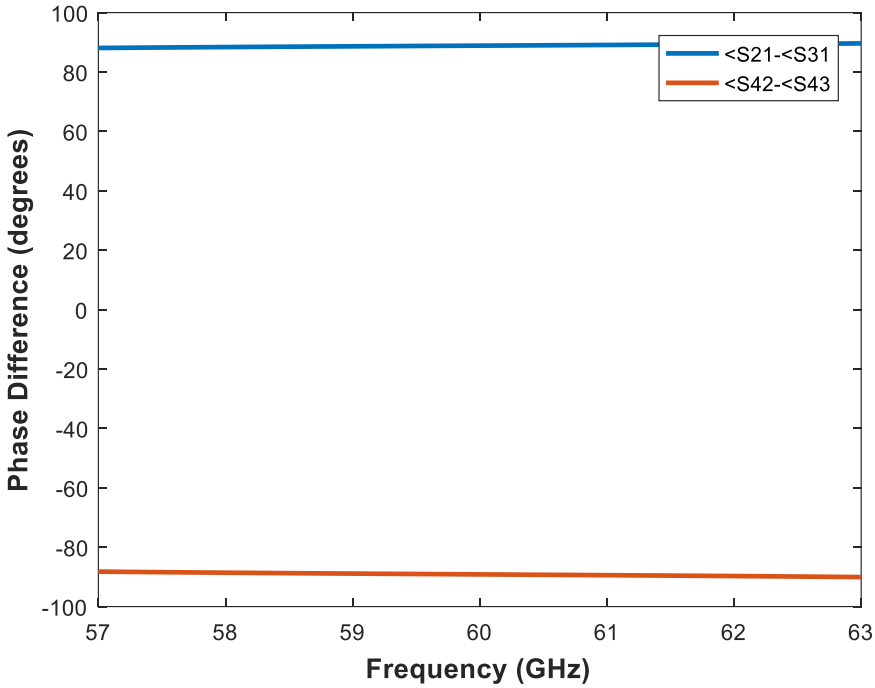


**Figure 7.9: Quadrature phase difference of the hybrid coupler in Figure 7.7.**

According to the metal density rules in the design rule manual, a continuous metal ground plane is not allowed at any metal layer. For this reason, the ground plane should be patterned accordingly in order to satisfy the design rules. Two extreme constraints are present: the first one imposes that the holes' dimensions should be at most equal to $\frac{\lambda_{eff}}{200}$. This therefore sets the maximum limit. The minimum limit is set by the design rules of the 90 nm industrial CMOS technology.

Figure 7.10 shows the 60 GHz hybrid coupler with a meshed ground plane, where both M1 (in blue) and M2 (in red) act as ground plane, where the latter shields more the silicon substrate. In fact, adding M2 on top of M1 with a $\frac{2w}{3}$ shift ($w$:metal width) improves the reflection at each port as well as the isolation at 60 GHz. Note that there are $\frac{w}{3} \times \frac{w}{3}\ \mu m^2$ holes in M1 layer with a $\frac{4w}{3}\ \mu m$ separation in both vertical and horizontal directions. The same case applies for M2 layer but with the holes shifted by $\frac{2w}{3}\ \mu m$ with respect to the holes in M1 layer.

Figure 7.11 shows the simulated S-parameters results in dB of the designed hybrid coupler with a meshed ground plane; where the RL is at least 14 dB at 60 GHz, presenting a good match at each port. The magnitude of $S_{41}$ shows that the isolation between port 1 and port 4 is higher than 18 dB at 60 GHz. Note that there is approximately a 1-dB magnitude imbalance between $S_{21}$ and $S_{31}$.

Figure 7.12 shows the quadrature phase difference in the outputs of the through and coupled arms of the hybrid coupler.

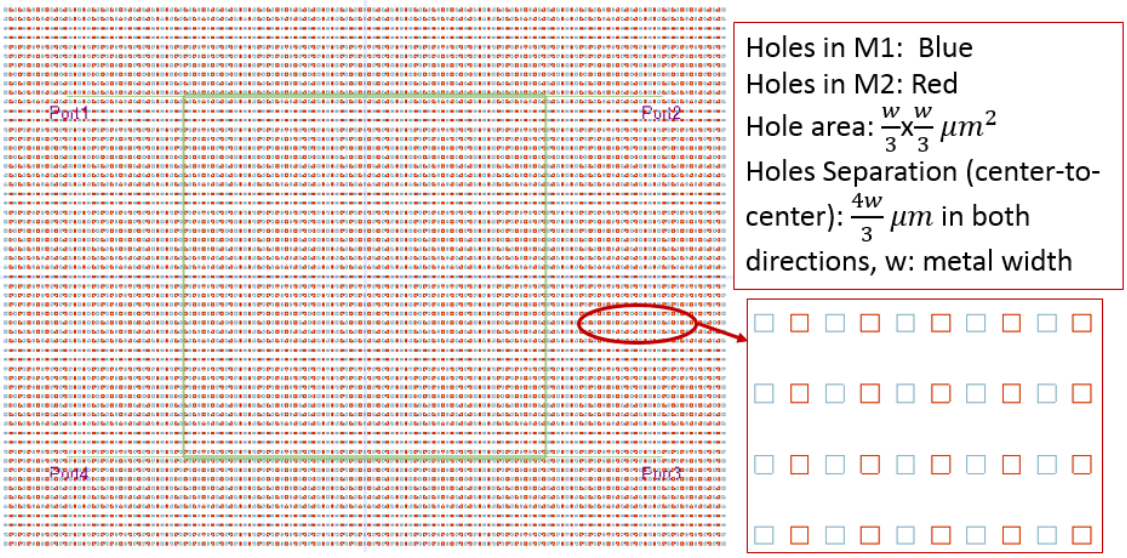


**Figure 7.10: 60 GHz hybrid coupler design with a meshed ground plane.**

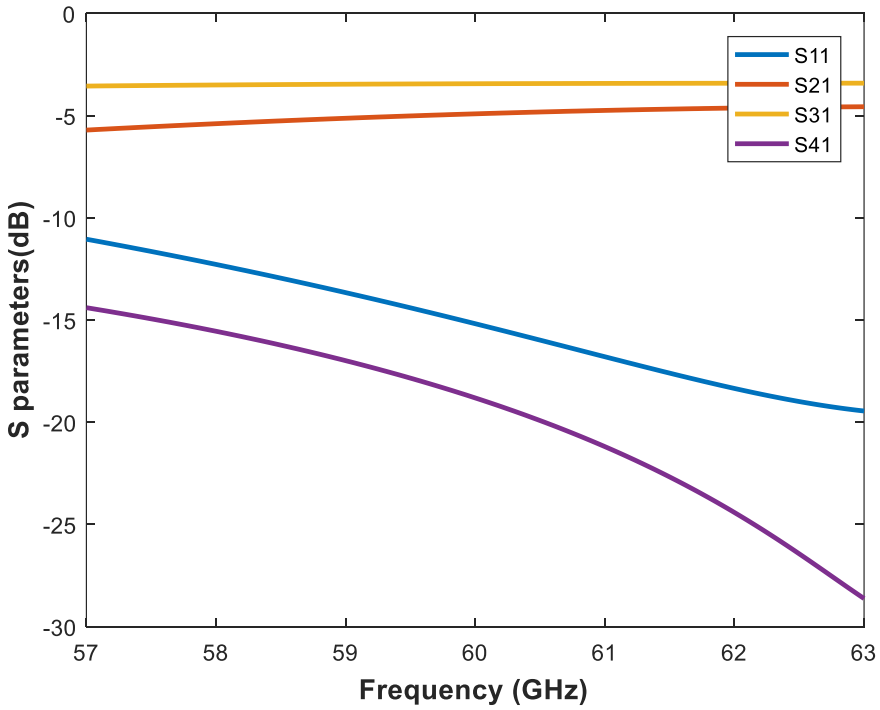


**Figure 7.11: Simulated S-parameters (dB) of the hybrid coupler in Figure 7.10.**

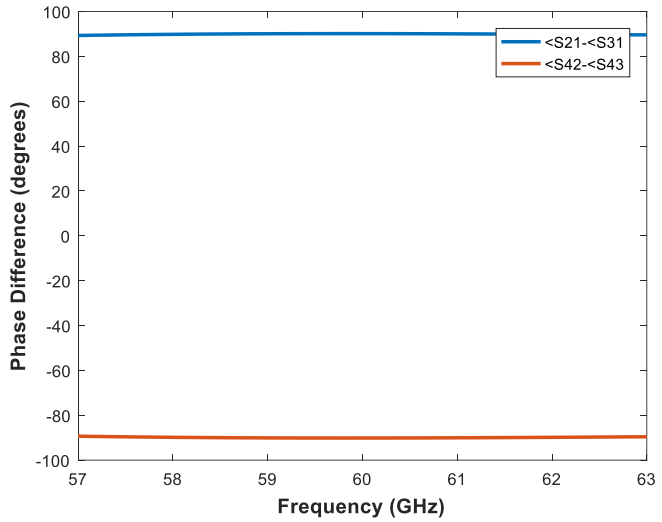


**Figure 7.12: Quadrature phase difference of the hybrid coupler in Figure 7.10.**

Figure 7.13 displays the final miniaturized design of the hybrid coupler in ADE HFSS 3D Layout, with a meshed ground plane (M1-M2 layers), operating at 60 GHz, and occupying an area of 0.35 $mm^2$; this represents a 48% reduction in the area compared to the design in Figure 7.7. The simulation results are shown in Figure 7.14 and Figure 7.15. Note that this design is key in the implementation of the overall phase shifter.

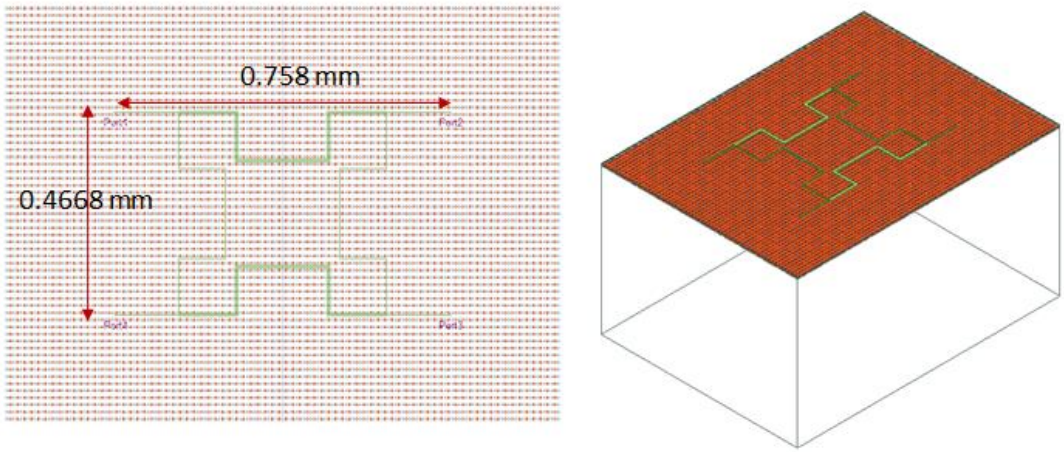


**Figure 7.13: Miniaturized design of the 60 GHz hybrid coupler with a meshed ground plane.**

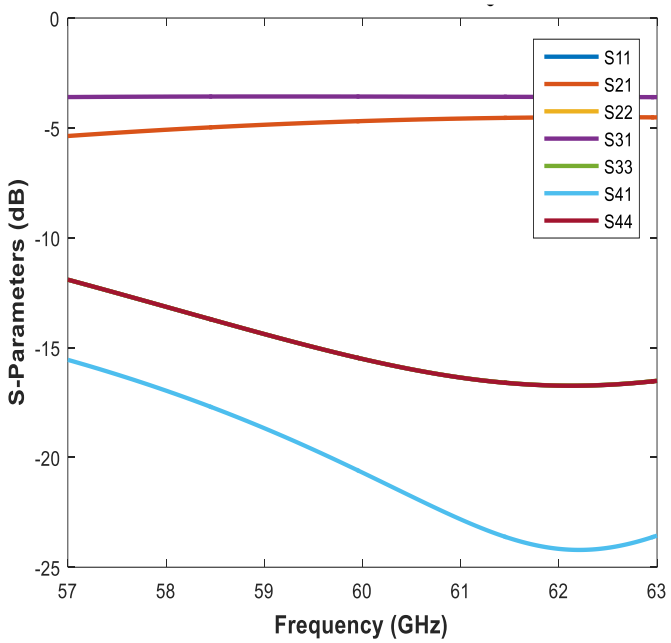


**Figure 7.14: Simulated S-parameters (dB) of the miniaturized hybrid coupler in Figure 7.13.**

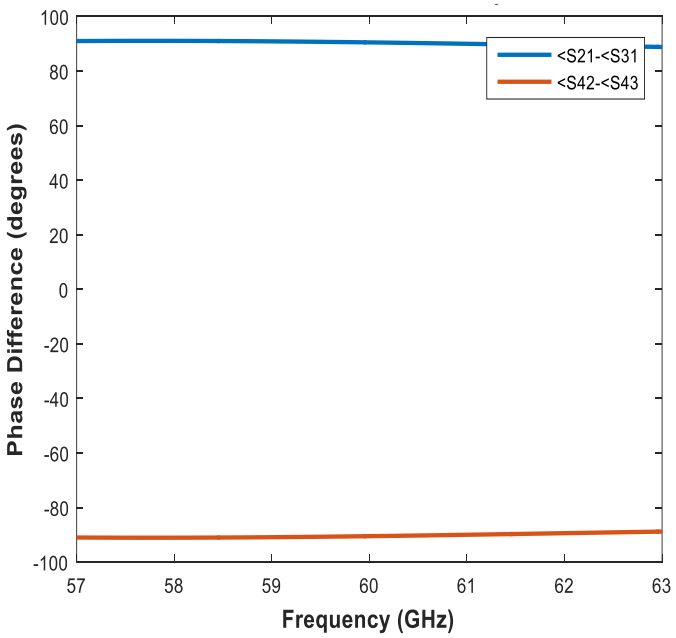


**Figure 7.15: Quadrature phase difference of the miniaturized hybrid coupler in Figure 7.13.**

## 7.5 Reflective Load

In this section, a new topology of the reflective load, which terminates both the through and the coupled ports of the 3-dB hybrid coupler, is presented at 60 GHz. First, a study of the MOS varactors employed in the design is completed at 60 GHz, followed by a presentation of previous topologies of the reflective load used in the literature, and finally the proposed topology of the reflective load is presented.

### *7.5.1 MOS Varactor Case Study*

We simulated the MOS varactors discussed earlier in section 4.2 to understand more their topology as well as their tuning range characteristics.

Figure 7.16 presents the circuit schematic of two varactors, the traditional D=S=B and the IMOS varactor, each implemented using a PMOS transistor and having the same design parameters. Note that Cadence Virtuoso platform [3] is used for the simulations.

The total MOSFET gate capacitance is composed of three components: the gate to source capacitance, the gate to drain capacitance and the gate to body capacitance, given by the following formula:

$$C_{gg} = C_{gs} + C_{gd} + C_{gb}$$

Figure 7.17 presents the capacitance range for both these topologies versus the tuning voltage at 60 GHz, showing that the IMOS varactor has higher capacitance ratio than the traditional D=S=B varactor.

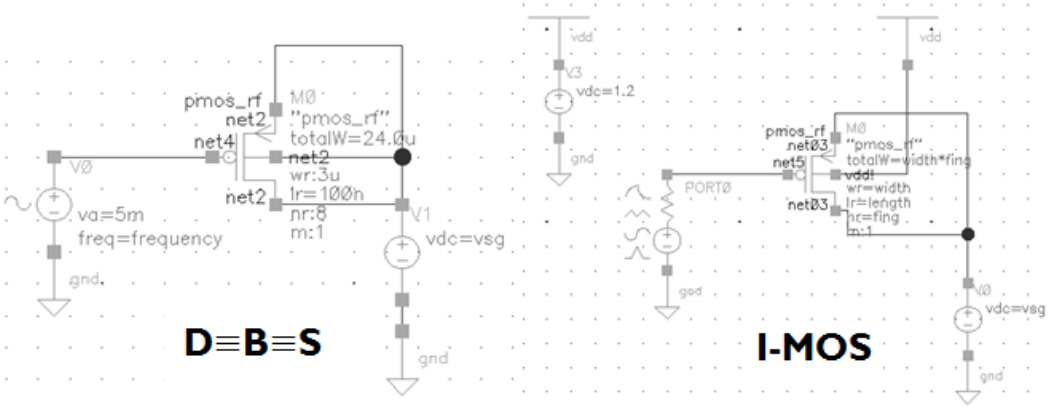


**Figure 7.16: D=S=B vs. IMOS varactors.**

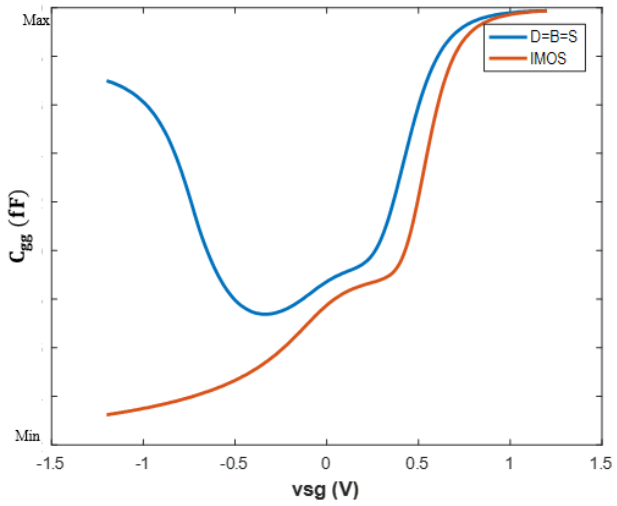


**Figure 7.17: Simulated capacitance versus voltage of D=S=B and IMOS varactors at 60 GHz.**

### 7.5.1.1 IMOS Analysis

In order to study the effect of each of the design parameters on the MOS varactor behavior at 60 GHz, especially its performance change with respect to its gate finger width, gate finger length and number of gate finger. A PMOS-based IMOS varactor is chosen as shown in Figure 7.16 to analyze such design parameters. Using the Analog Design Environment (ADE) in Cadence Virtuoso platform, the transistor design

parameters are swept within the limits imposed by the technology, and the IMOS C-V characteristics are plotted for each parameter sweep, while keeping the others fixed.

The oxide capacitance is proportional to the area of the device, hence increasing the device width or length increases the capacitance value.

Increasing the number of gate fingers or the gate finger width, increases the oxide capacitance, which leads to an increase in the capacitance value as shown in Figure 7.18 and Figure 7.19.

Figure 7.20 shows that as the gate finger length increases, the varactor tuning range increases as well.

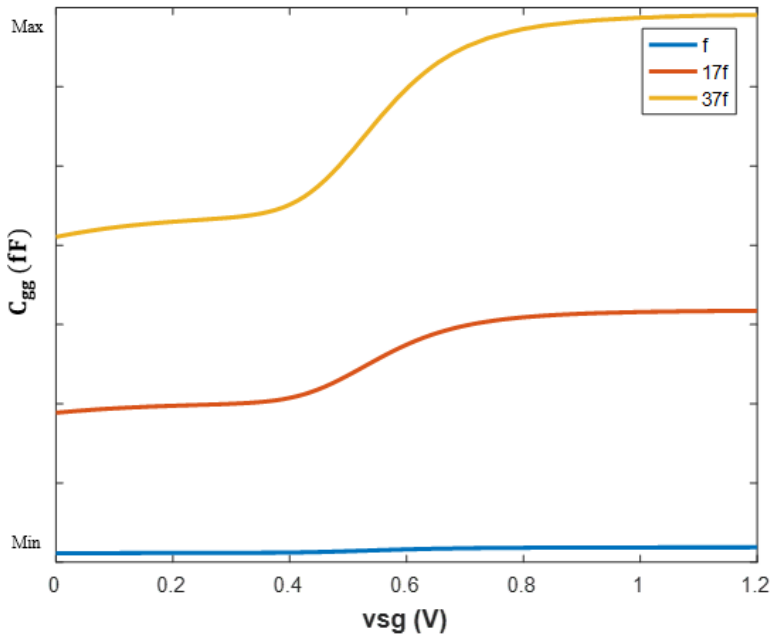


**Figure 7.18: Effect of varying the number of gate finger (f) on the IMOS C-V characteristic at 60 GHz.**

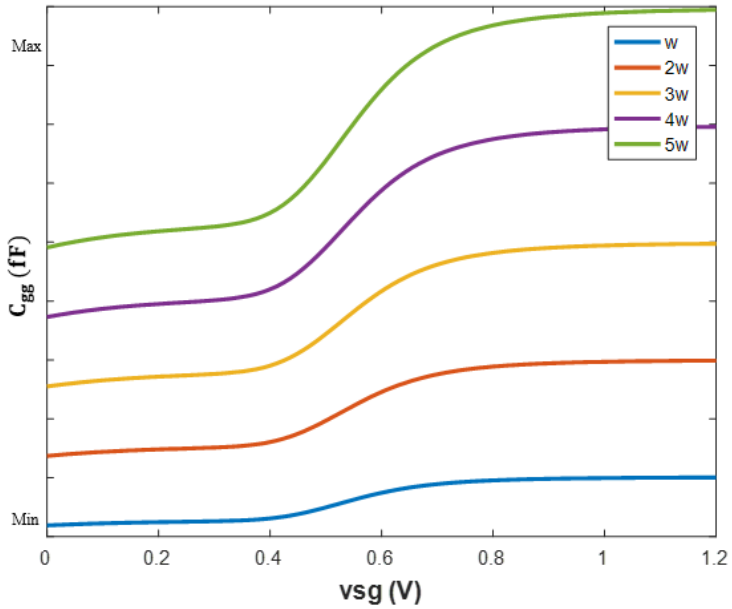


**Figure 7.19: Effect of varying the gate finger width (w) on the IMOS C-V characteristic at 60 GHz.**

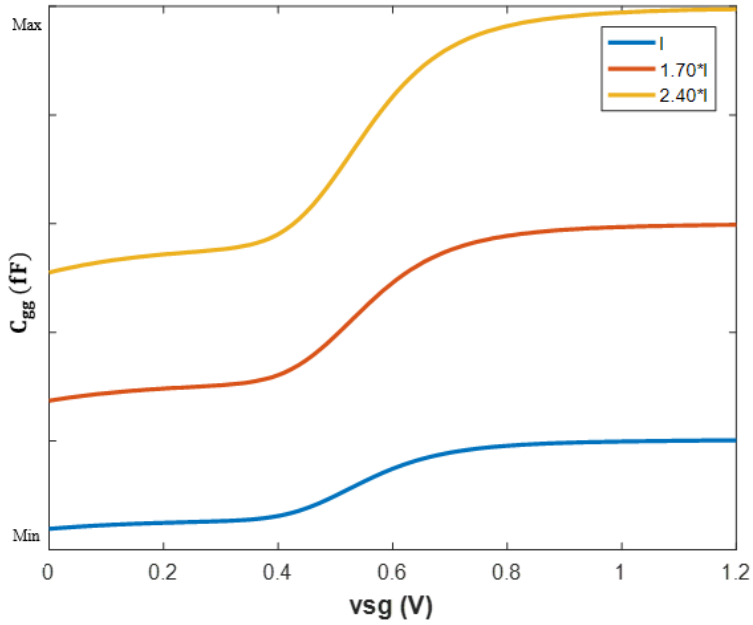


**Figure 7.20: Effect of varying the gate finger length (l) on the IMOS C-V characteristic at 60 GHz.**

The IMOS varactor shown in Figure 7.16 achieves a maximum phase range of 54° at 60 GHz while having the following dimensions: a gate finger length of 240 nm, a

gate finger width of 4 $\mu$m, and a number of gate finger of 5. However, this results in a high loss variation of 2.73 dB across the tuning voltage. This is illustrated in Figure 7.21 where the simulated phase shift and the magnitude of the reflection coefficient (loss) are plotted versus the bias voltage.

Figure 7.22 shows the variation of the capacitance and the resistance across the tuning voltage. Note that the varactor features a high series resistance and a capacitance ratio of approximately 2.

Another representation of the varactor loss across tuning voltage at 60 GHz is shown on the smith chart in Figure 7.23. Ideally, assuming a lossless varactor, the reflection coefficient trace should be along the outer unit circle of the smith chart; however, due to the high varactor parasitic resistance, the trace is shifted toward the center of the smith chart.

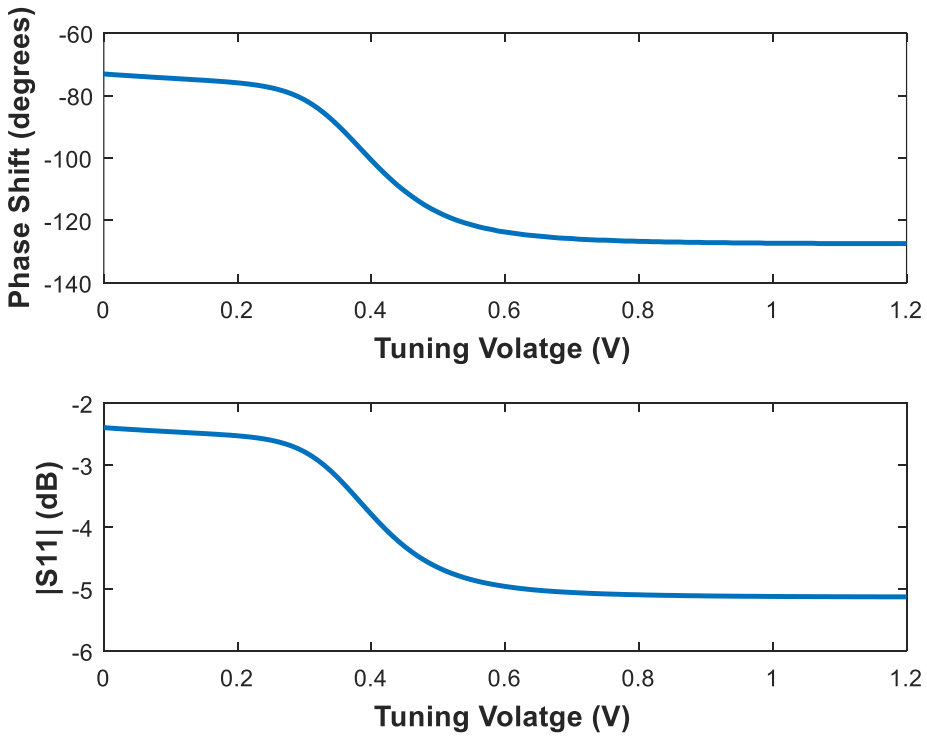


**Figure 7.21: Simulated phase shift (degrees) and reflection coefficient (dB) versus tuning voltage of IMOS varactor at 60 GHz.**

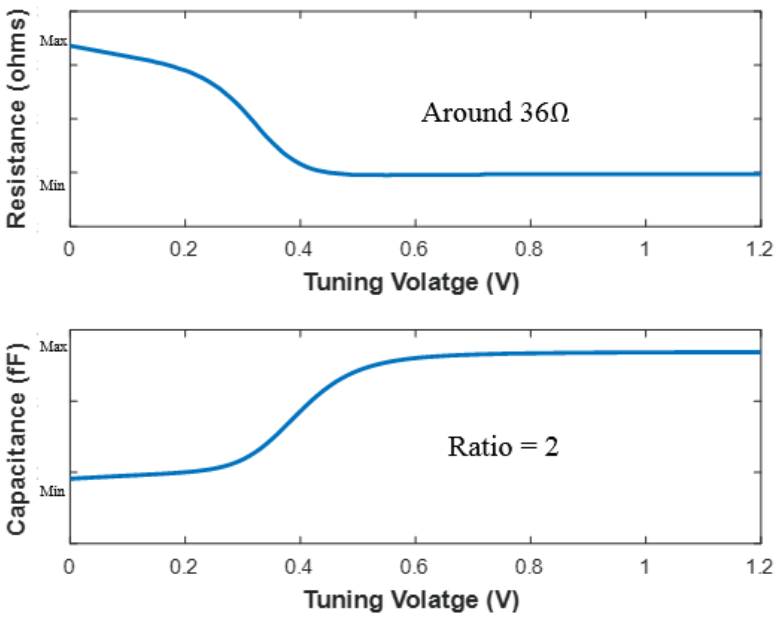


**Figure 7.22: Simulated resistance and capacitance versus tuning voltage of IMOS varactor at 60 GHz.**

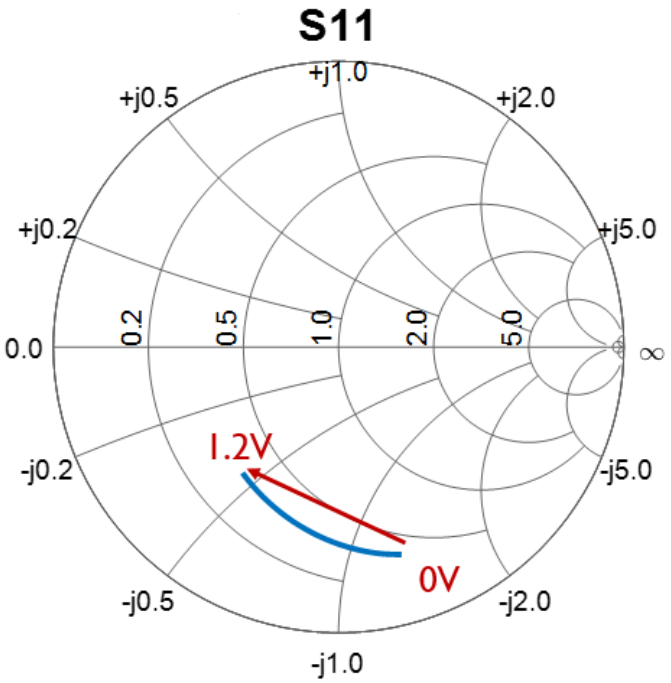


**Figure 7.23: IMOS reflection coefficient variation across tuning voltage at 60 GHz.**

At mm-wave frequencies, the quality factor of the reflective load is limited by the varactor performance and not by that of the inductor. It is given by the ratio of the stored energy to the energy loss, in other terms, the ratio of the reactive impedance part to the resistive one.

As shown in Figure 7.24, the simulated Q-factor of the IMOS varactor is plotted versus frequency and as function of the tuning voltage. The graph shows that the IMOS varactor presents a very low Q-factor, due to its high resistive losses as shown previously.

The minimum and maximum Q-factor versus the gate finger length are retrieved for the IMOS varactor at 60 GHz as shown in Figure 7.25. It is demonstrated that very low values that are less than 10 render the varactors unsuitable for mm-wave frequencies [58]. Note that the Q-factor of the varactors increases with smaller gate lengths and lower n-well sheet resistance.

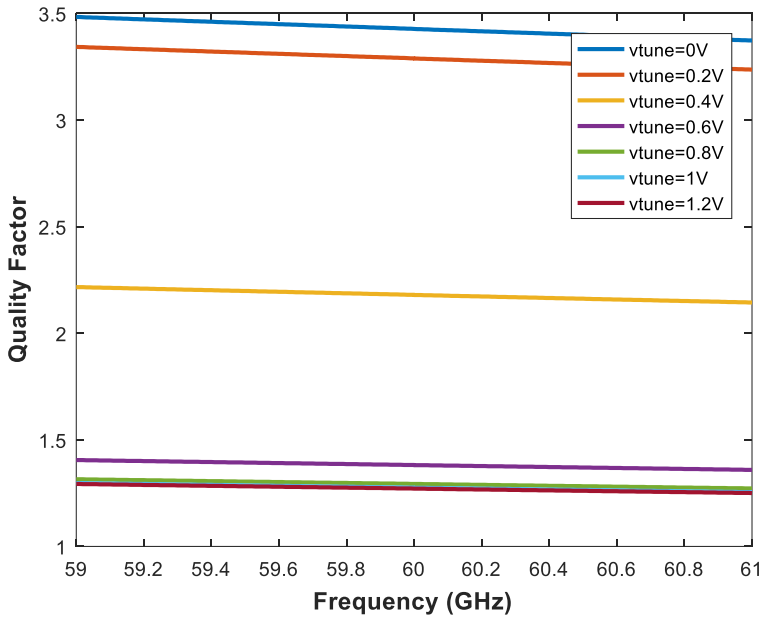


**Figure 7.24: Simulated normalized Q-factor versus frequency and across tuning voltage of the IMOS varactor.**

The capacitance ratio of the IMOS varactor at 60 GHz is plotted versus the gate finger length while varying the gate finger width as shown in Figure 7.26.

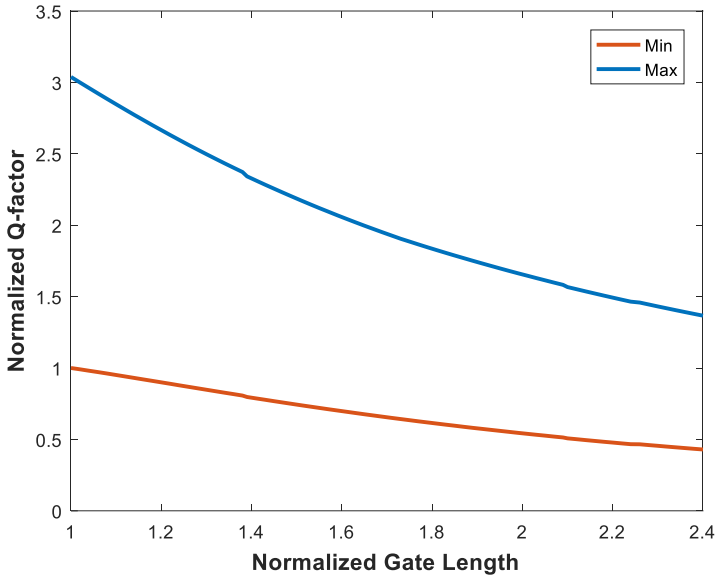


**Figure 7.25: Minimum and maximum Q-factor versus gate finger length of the IMOS varactor at 60 GHz.**

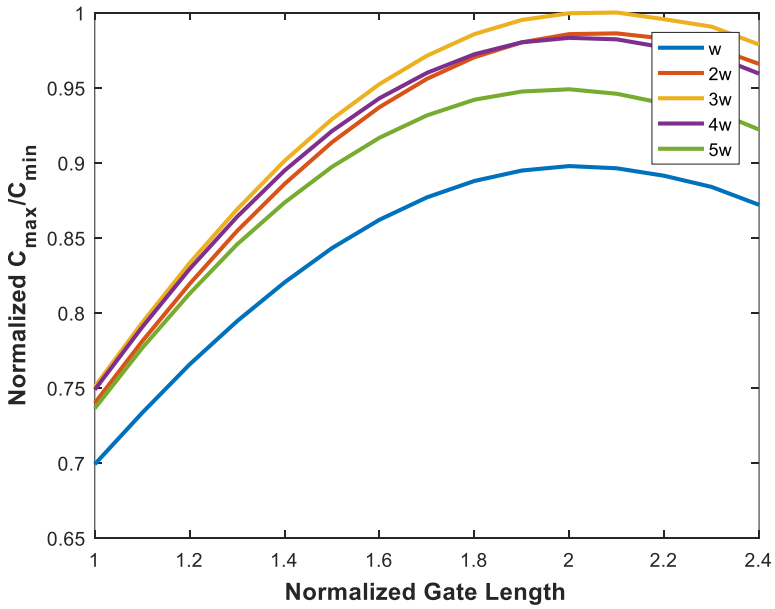


**Figure 7.26: Capacitance ratio versus gate finger length and across the gate finger width of the IMOS varactor at 60 GHz.**

#### 7.5.1.2 AMOS Analysis

In the previous parts, the analysis focused on studying the IMOS varactor. To address the shortcomings of the IMOS varactors, an AMOS-based varactor is chosen from the 90nm industrial technology library in order to study its performance and characteristics.

The minimum and maximum Q-factor versus the gate finger length, in the allowed sweep range, are retrieved for the AMOS varactor at 60 GHz as shown in Figure 7.27. The Q-factor achieved by the AMOS varactor is relatively higher than that reached by the IMOS varactor, and this is mainly due to the high doping density of the channel. Such performance implies a very low parasitic resistance at mm-wave frequencies [59].

The capacitance ratio of the AMOS varactor at 60 GHz is plotted against the gate finger length while varying the gate finger width as shown in Figure 7.28. Such ratio reaches a maximum more than three times higher than that of the IMOS varactor, hence featuring higher capacitance range. For this reason, we relied on AMOS-based varactors used in the proposed reflective load.

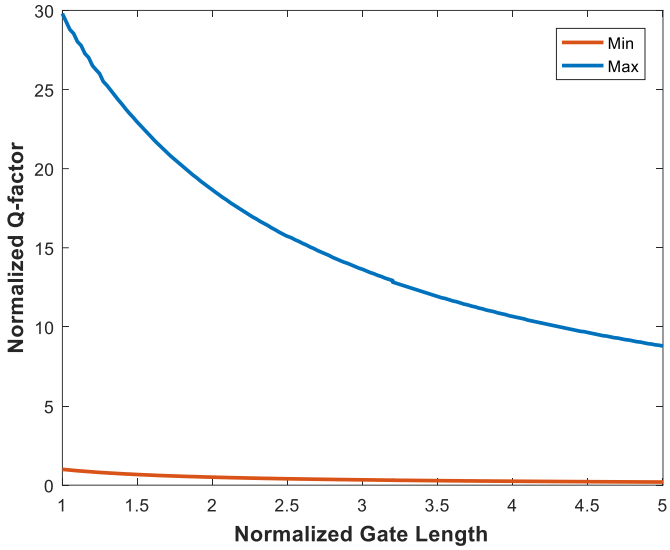


**Figure 7.27: Minimum and maximum Q-factor versus gate finger length of the AMOS varactor at 60 GHz.**

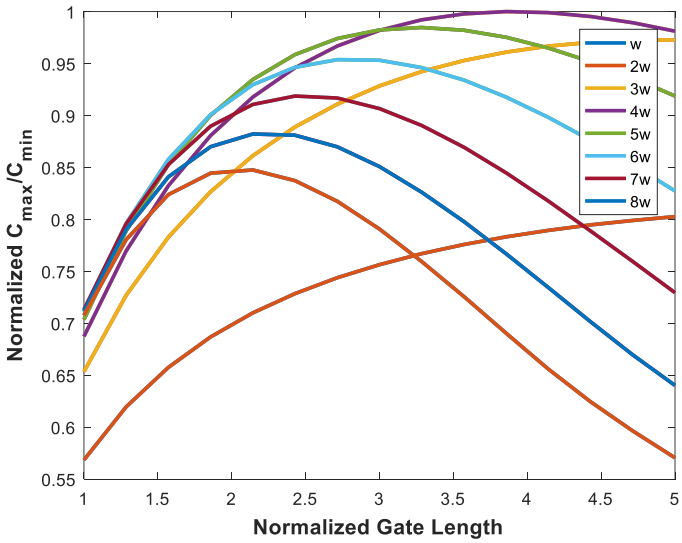


**Figure 7.28: Capacitance ratio versus gate finger length and across the gate finger width of the AMOS varactor at 60 GHz.**

Figure 7.29 presents the phase range as function of the AMOS varactor dimensions, while the loss variation is shown in Figure 7.30. It can be concluded that seeking a maximum phase range may result in a very high loss variation across the tuning voltage. Therefore, a search for an optimal design point is needed.

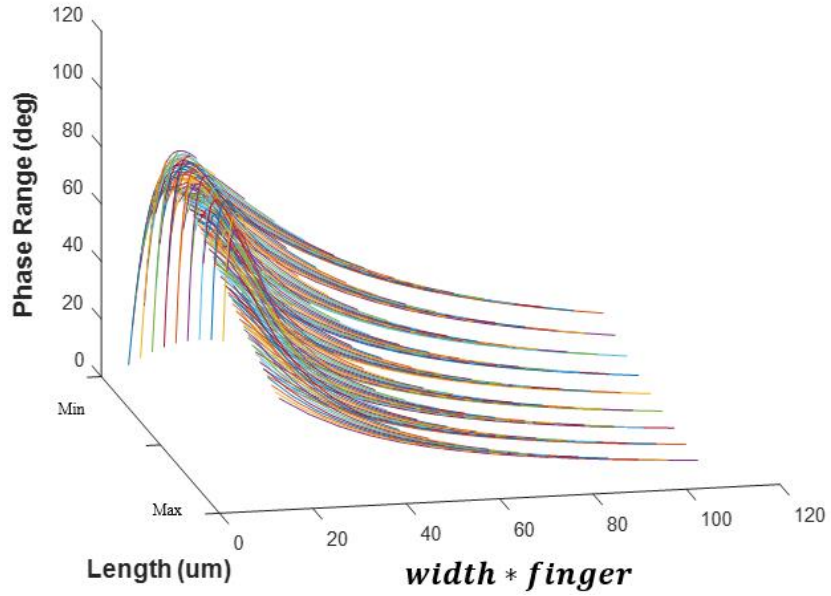


**Figure 7.29: Phase range variation as function of the AMOS varactor dimensions: gate finger length and gate width.**

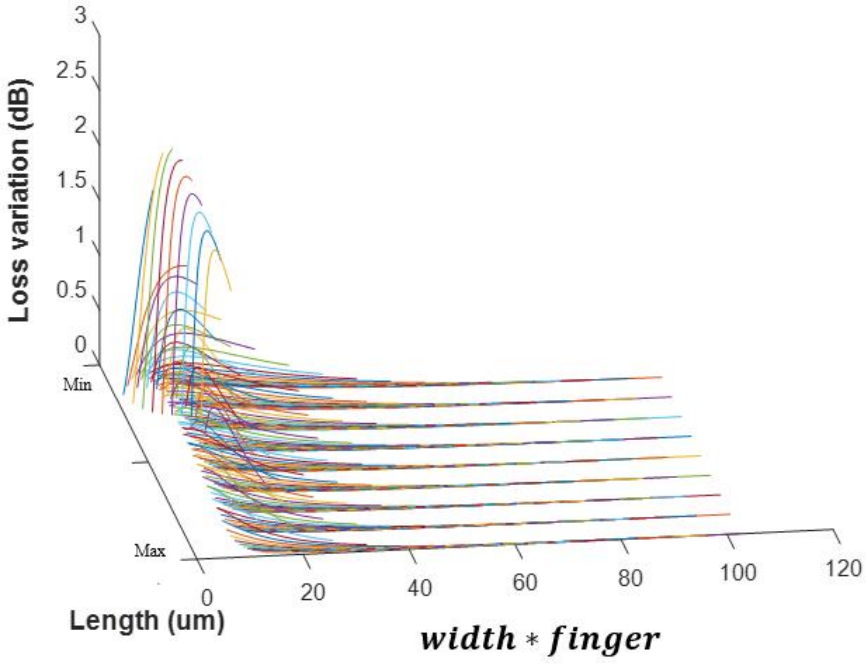


**Figure 7.30: Loss variation as function of the AMOS varactor dimensions: gate finger length and gate width.**

Figure 7.31 shows the loss versus frequency of a given AMOS varactor, which reaches a maximum at 60 GHz.

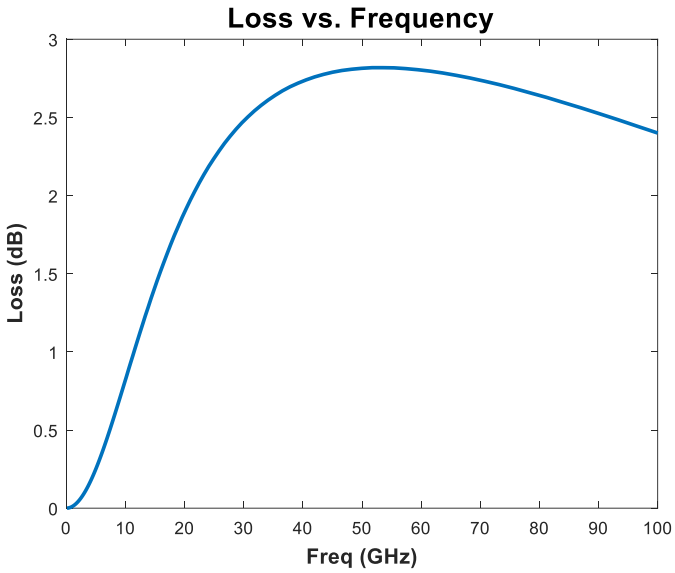


**Figure 7.31: Loss variation versus frequency of AMOS varactor.**

### *7.5.2 Overview of Reflective Load Topologies in Literature*

Several topologies of reflective loads have been recently proposed, each achieving different tuning ranges. For instance, the capacitive load, such as a single varactor, has a typical maximum tuning range of 60° in practice due to passive losses in silicon process [60]. Note that in 90 nm industrial technology and chosen device sweep ranges, the AMOS-based varactor reaches theoretically a maximum tuning range of 100°, twice that the maximum achieved by the IMOS varactor. Another topology is the series L-C resonant load, where in this case, a zero is achieved, and a maximum tuning of 120° is reached [60]. The same applies for the parallel L-C resonant load, which achieves a parallel resonance (a pole) instead of a series one. Both parallel and series L-C loads are 2$^{nd}$ order resonators achieving only one resonance, however, in order to get

large phase shift variations, a high-order reflective load with multiple resonances is needed. In other terms, the load impedance trajectory on the smith chart can be extended by covering multiple short-circuit (S.C) and open-circuit (O.C.) resonance points as shown in Figure 7.32. A triple symmetric resonating load presented previously [34] in Figure 3.15 can achieve a 360° full phase range.

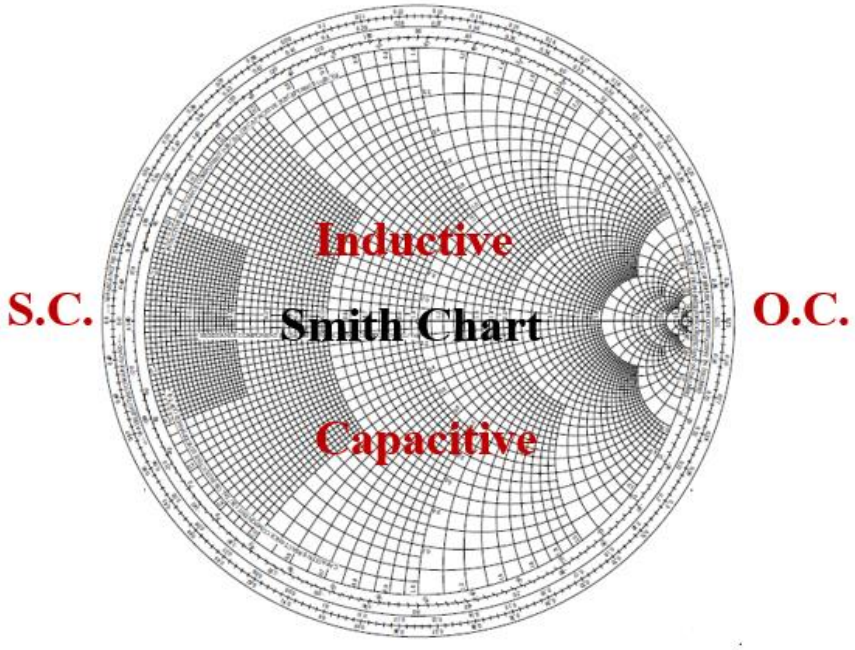


**Figure 7.32: Resonance concept for reflective loads illustrated on the smith chart.**

Figure 7.33 presents a snapshot of the discussed topologies with the simulated results of their phase shifting range on the smith chart that were extracted using ADS, assuming lossless elements [54].

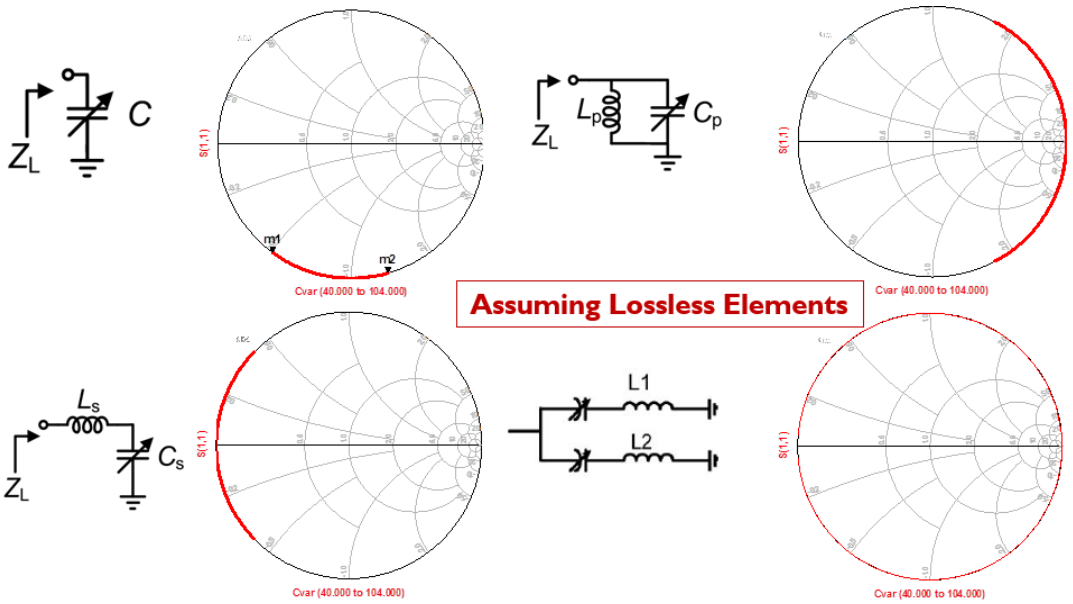


**Figure 7.33: Previous topologies of reflective load used in loading the RTPS.**

### *7.5.3 Proposed Topology of the Reflective Load*

A fourth order asymmetric reflective load is proposed to be used in terminating both the through and the coupled ports of the hybrid coupler. It is composed of two differently sized AMOS-based varactors and two inductors as shown in Figure 7.34. Compared to the symmetric topology presented in [34], the asymmetric topology achieves higher phase variation based on our case studies implemented in the 90nm industrial technology.

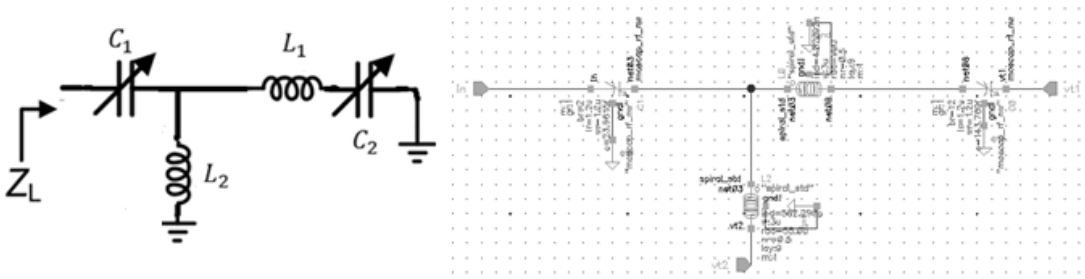


**Figure 7.34: New topology for the reflective load and its schematic in Cadence Virtuoso platform.**

Looking at either the through or the coupled port of the RTPS, the load impedance is given by the following expression assuming lossless passive components (varactors and inductors):

$$Z_L = j[\frac{\omega^2 L_2 C_1(\omega^2 L_1 C_2 - 1) + \omega^2 C_2(L_1 - L_2) - 1}{\omega C_1[\omega^2 C_2(L_1 + L_2) - 1]}]$$

The proposed reflective load can cover theoretically up to three resonance points alternating between S.C and O.C. The analysis starts by the following:

- $L_1$-$C_2$ forms a series resonance, the load impedance $Z_L$ is fully determined by $C_1$. By varying $C_1$, the lower left part of the unit circle on the smith chart can be covered.
- As $C_2$ increases, the $L_1$-$C_2$ series resonator becomes inductive, which can combine with $L_2$ to form a series resonance with $C_1$ to realize a S.C. load, assuming that $C_1$ is tuned to its maximum value.
- As $C_2$ decreases, the $L_1$-$C_2$ becomes capacitive which will form a parallel resonance with $L_2$, forming an O.C.
- As $C_2$ further decreases, the $L_2$-$L_1$-$C_2$ becomes inductive leading to a series resonance with $C_1$ forming a S.C., assuming that $C_1$ is tuned to its minimum value.

The above points impose the following condition: $C_{1,min} > C_{2,min}$. This can be achieved in two ways: either controlling the varactors independently, i.e. different tuning voltages, or sizing the varactors differently. The latter way is chosen to avoid the need for two independent circuitries.

Table 7.1 summarizes the achieved resonances by the newly proposed reflective load.

**Table 7.1: Achieved resonances by the new proposed reflective load**

| | **$L_1$ s $C_2$** | **$C_1$ s ($L_1$//$L_2$) Series resonance** | **$L_2$//$C_2$ Parallel resonance** | **$C_1$ s $L_2$ Series resonance** |
|---|---|---|---|---|
| **$Z_L$** | Variable $C_1$ | S.C. | O.C. | S.C. |
| **$C_1$** | | $C_{1,max}$ | | $C_{1,min}$ |
| **$C_2$** | | $C_{2,max}$ | $C_{2,min} < C_2 = C_{1,min} < C_{2,max}$<br>$C_{1,min} > C_{2,min}$ | $C_{2,min}$ |

As shown previously in Figures 7.29 & 7.30, there is a tradeoff between the maximum phase range and the loss variation across the tuning voltage. For this reason, an exhaustive search is done in order to find the optimal point.

In the proposed reflective load, the two AMOS-based varactors are tuned with the same control voltage in the range of -1V to 0.5V but sized differently. The varactor $C_1$ has the following dimensions: a gate finger length of 1.2 $\mu$m, a gate finger width of 1.2 $\mu$m, and a number of gate fingers of 2. The varactor $C_2$ has the same gate finger width and length, but with a number of gate fingers of 12. Note that the previous condition on the minimum value of the capacitors does not hold anymore due to the compromise added on the phase shift range.

The inductors have been chosen from the technology library using parameterized cells (Pcells). A half-turn inductor occupying $322\ \mu m \times 319\ \mu m$ is used to implement $L_1$, while $L_2$ is a half-turn inductor occupying $252\ \mu m \times 249\ \mu m$. One drawback is that the inductors have large footprints and occupy an area of around 0.16 $mm^2$.

Figure 7.35 presents the layout of the proposed reflective load in Cadence Virtuoso platform, occupying an area of 0.22 $mm^2$ and meeting the design rules of the 90nm industrial CMOS technology.

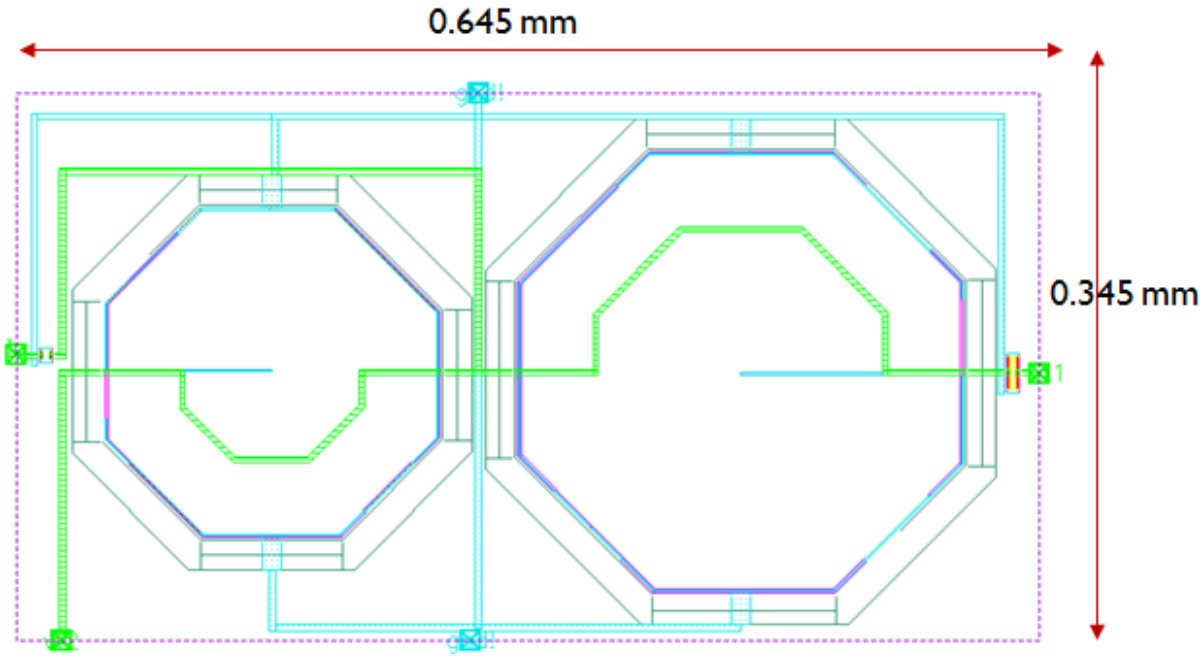


**Figure 7.35: Layout view of the new reflective load in Cadence Virtuoso platform.**

Figure 7.36 shows the phase range achieved by the proposed reflective load across the control voltage where $\Delta\varphi = 241°$.

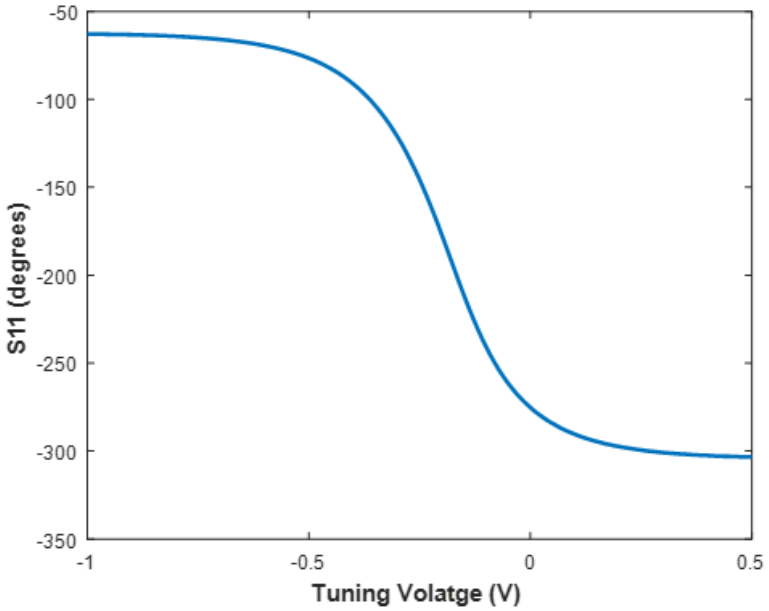


**Figure 7.36: Phase shift versus control voltage for the proposed reflective load.**

Figure 7.37 shows the loss variation caused by the proposed reflective load across the control voltage where it reaches around 6 dB. This is mainly due to the parasitic resistance of the reflective load. This leads to a FoM of 41°/dB.

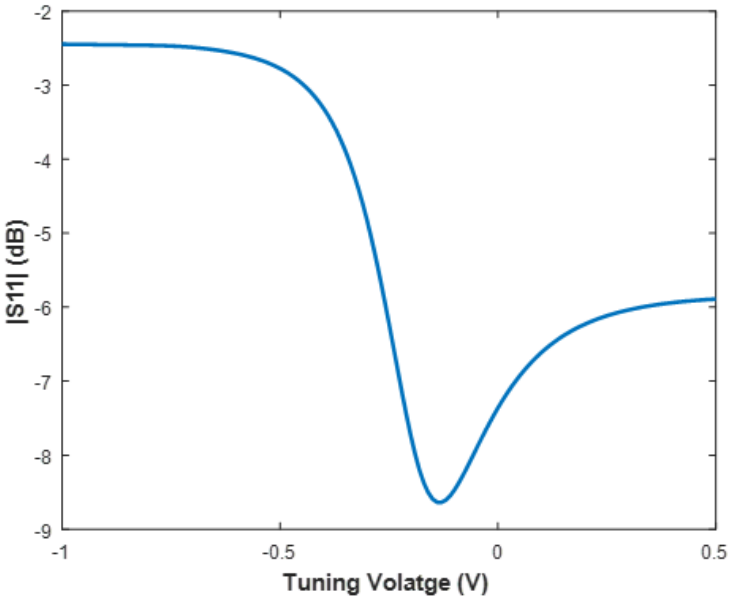


**Figure 7.37: Loss versus control voltage for the proposed reflective load.**

### *7.5.4 Discussion*

In order to compare the behavior of the proposed reflective load implemented in the underlying technology to other topologies present in the literature which were presented in section 7.5.2, simulations are performed in Cadence Virtuoso for the various load configurations at 60 GHz, where both the phase shift and loss are plotted versus the tuning voltage. Note that the AMOS-based varactor is used in all these topologies.

Figure 7.38 shows the phase shift and loss variation for the AMOS-based varactor at 60 GHz, where $\Delta\varphi = 103.9°$ and $\Delta loss = 2.806\ dB$, leading to a FoM of 37°/dB. Note that this is the maximum achieved phase range for a single varactor.

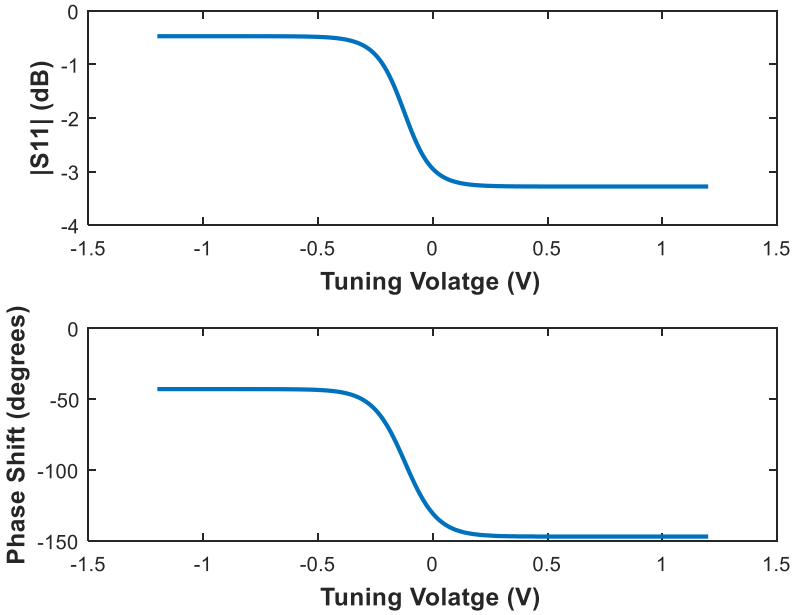


**Figure 7.38: Phase shift and loss versus control voltage for the AMOS-based varactor load.**

Figure 7.39 shows the phase shift and loss variation for the parallel L-C resonant load at 60 GHz, where $\Delta\varphi = 198.75°$ and $\Delta loss = 5.689\ dB$, leading to a FoM of 35°/dB.

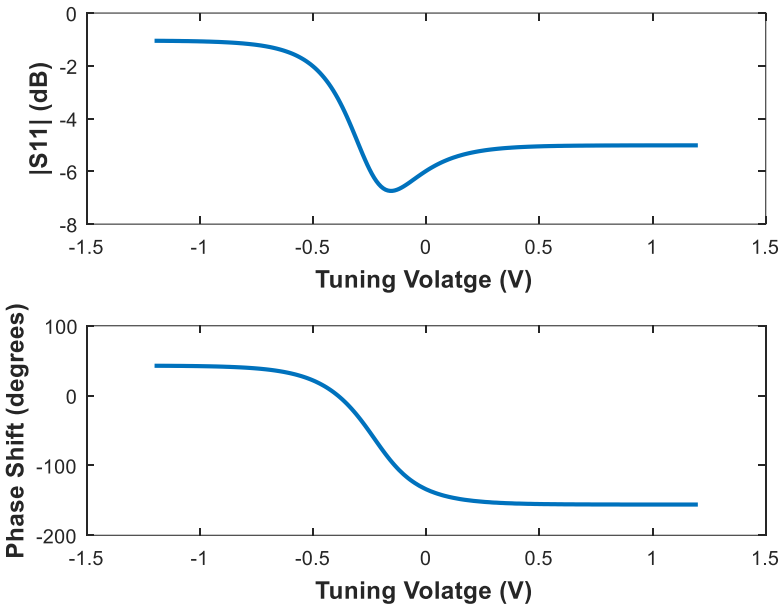


**Figure 7.39: Phase shift and loss versus control voltage for the parallel L-C resonant load.**

Figure 7.40 shows the phase shift and loss variation for the series L-C resonant load at 60 GHz, where $\Delta\varphi = 150.3°$ and $\Delta loss = 5.353\ dB$, leading to a FoM of 28°/dB.

Figure 7.41 shows the phase shift and loss variation for the triple resonating load at 60 GHz, where $\Delta\varphi = 127.5°$ and $\Delta loss = 5.612\ dB$, leading to a FoM of 23°/dB.

As can be concluded, the proposed reflective load surpasses the other topologies by achieving a FoM of around 41°/dB, and specifically shows a better performance than the 4$^{th}$ order triple resonating load which only achieves a phase range of $127.5°$ given the same loss variation.

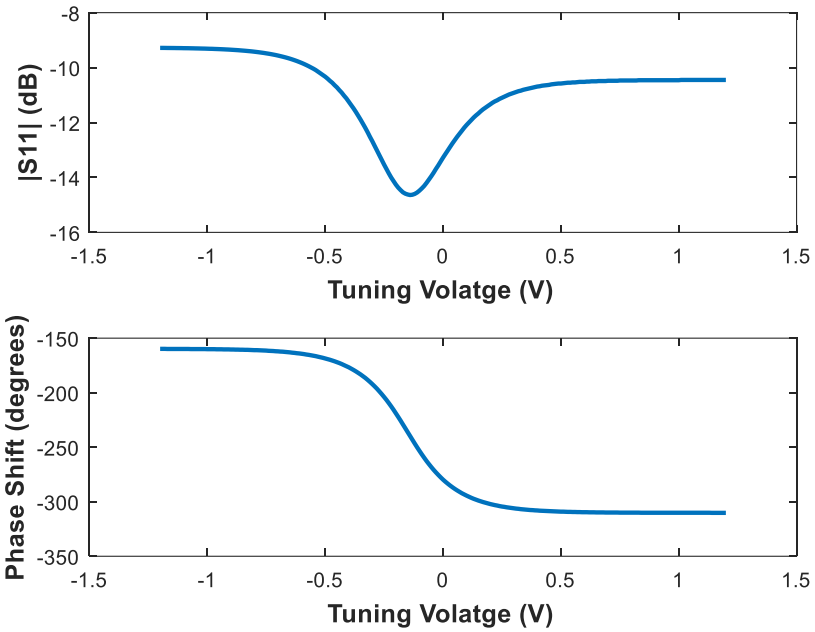


**Figure 7.40: Phase shift and loss versus control voltage for the series L-C resonant load.**

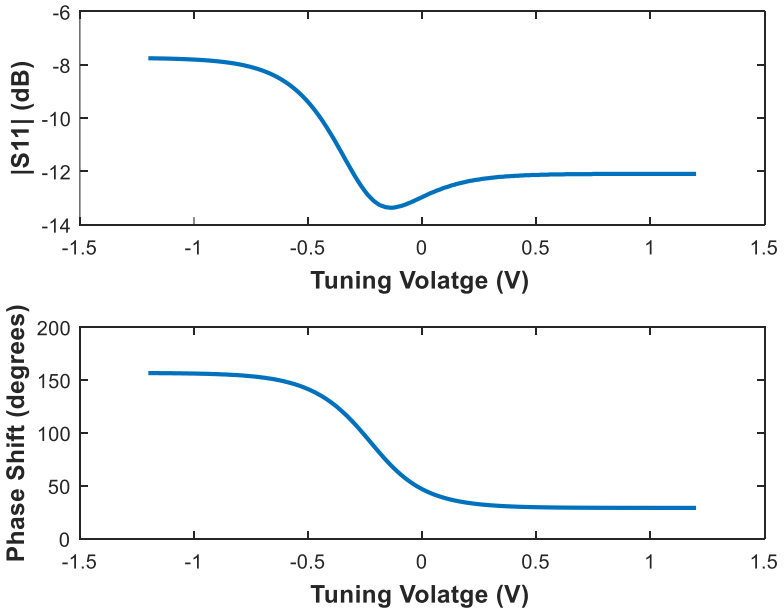


**Figure 7.41: Phase shift and loss versus control voltage for the triple resonating load.**

## 7.6 Overall Phase Shifter

In this section, the overall RTPS is presented in terms of its design and characteristics. First, we provide a quick review emphasizing relevant characteristics and complementing the introductory RTPS discussion presented earlier in section 3.3.3.

### *7.6.1 Theory of Operation*

As shown in Figure 7.1, the reflection coefficient at the through and coupled ports $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$ is a major player in determining the characteristics of the phase shifter. The variation of its phase determines the RTPS phase shift range, and its magnitude represents the loss introduced by the reflective load. Our main goal is to enable a full range phase shifter for phased array applications. This can be achieved by maximizing the reflection coefficient phase range while minimizing its magnitude variation.

The RTPS phase shift from the input to the isolated port is controlled by varying the impedance of the reflective load and is given by:

$$\varphi = -\frac{\pi}{2} - 2\tan^{-1}(\frac{X}{Z_0})$$

where X is the reactance of the reflective load and $Z_0$ is the characteristic impedance of the hybrid coupler. The RTPS phase shift range can be computed according to the following equation.

$$\Delta\varphi = 2[\tan^{-1}\left(\frac{X_{max}}{Z_0}\right) - \tan^{-1}\left(\frac{X_{min}}{Z_0}\right)]$$

where $X_{min}$ and $X_{max}$ represent the lower and upper bounds for the range of X.

In order to get high phase variations, the variable load should be purely reactive, and this translates to having high quality factor Q. However, some losses are still recorded. The RTPS insertion loss includes two components: the hybrid coupler

losses as well as the parasitic losses of the reflective loads, and it is expressed by: $IL_{RTPS}(dB) = 2IL_{coupler} + |\Gamma|$.

In order to achieve wide phase-shifting range, several methods are employed such as cascading multiple RTPS designs that exhibit exceedingly high IL, or by employing a high-order reflective load [60] instead of a single varactor as shown previously.

In spite of its small size, simple design and simple controlling scheme, RTPS may suffer from a large insertion loss variation across the phase control range. The main sources of this disadvantage are the varactors in the reflective load as discussed in Section 7.5.1 due to the degradation in their Q-factor.

### *7.6.2 Proposed Design: Implementation and Results*

The schematic of the overall phase shifter is shown in Figure 7.42 using Cadence Virtuoso platform. A co-simulation between ADE HFSS 3D Layout and Cadence Virtuoso is performed. The EM-simulation results of the 100Ω hybrid coupler are exported from ADE HFSS and integrated inside Cadence Virtuoso using a 4-port symbol (SnP file) representing the S-parameters of the hybrid coupler.

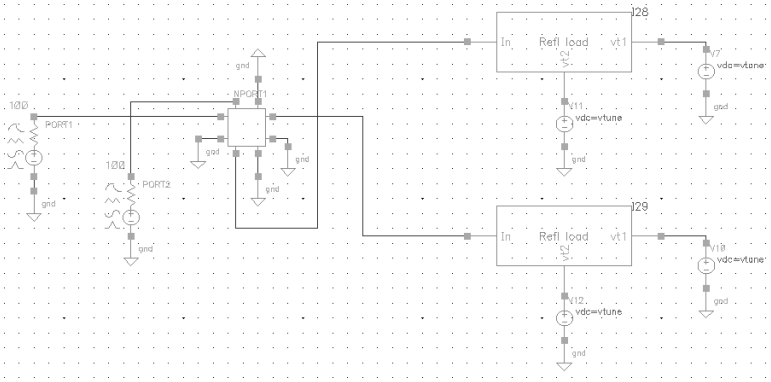


**Figure 7.42: Schematic view of the overall phase shifter in Cadence Virtuoso platform.**

Figure 7.43 presents the layout of the overall phase shifter in Cadence Virtuoso platform, illustrating the branch-line coupler loaded by two identical reflective loads, occupying an area of 1.12 $mm^2$ and meeting the design rules of the 90nm industrial CMOS technology.

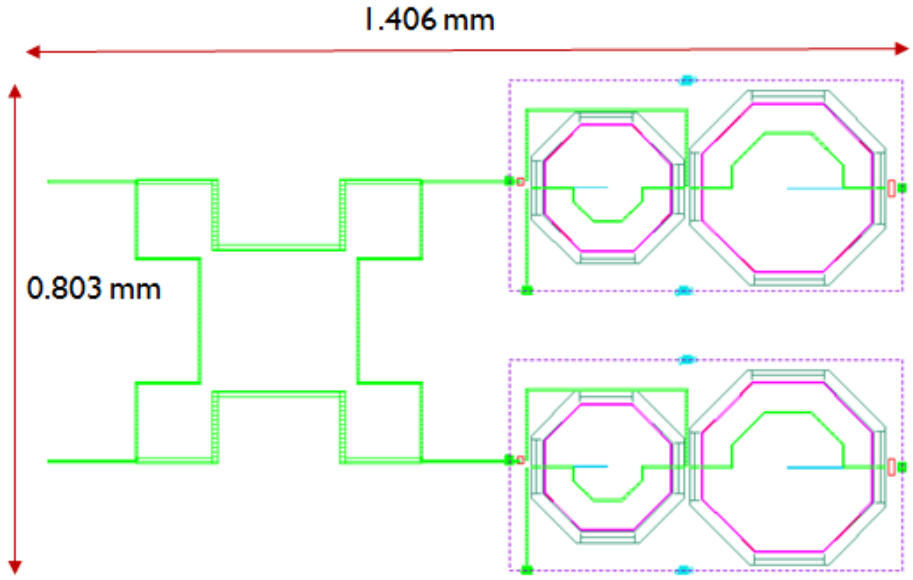


**Figure 7.43: Layout view of the overall phase shifter in Cadence Virtuoso platform.**

Figure 7.44 shows the trajectory of the transmission coefficient $S_{21}$ of the overall phase shifter on the smith chart. The RTPS achieves a maximum phase range of 254°. This is also shown in Figure 7.45 where the span of the phase shift is plotted versus frequency for various tuning voltages.

Figure 7.46 presents the RTPS insertion loss versus frequency across the control voltage. It is clear that there is around 5 dB loss variation at 60 GHz across the tuning range. This can be compensated by the use of variable gain amplifiers in the phased array transceiver chain.

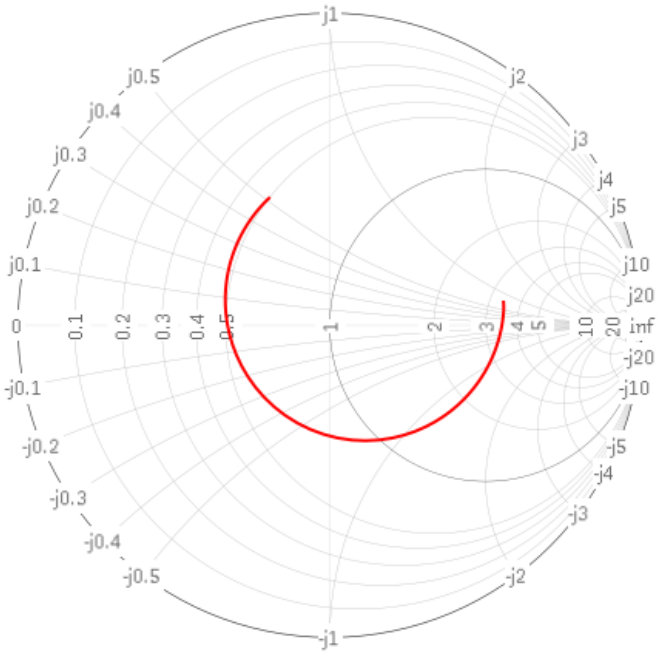


**Figure 7.44: Transmission coefficient $S_{21}$ of the overall phase shifter illustrated on the smith chart.**

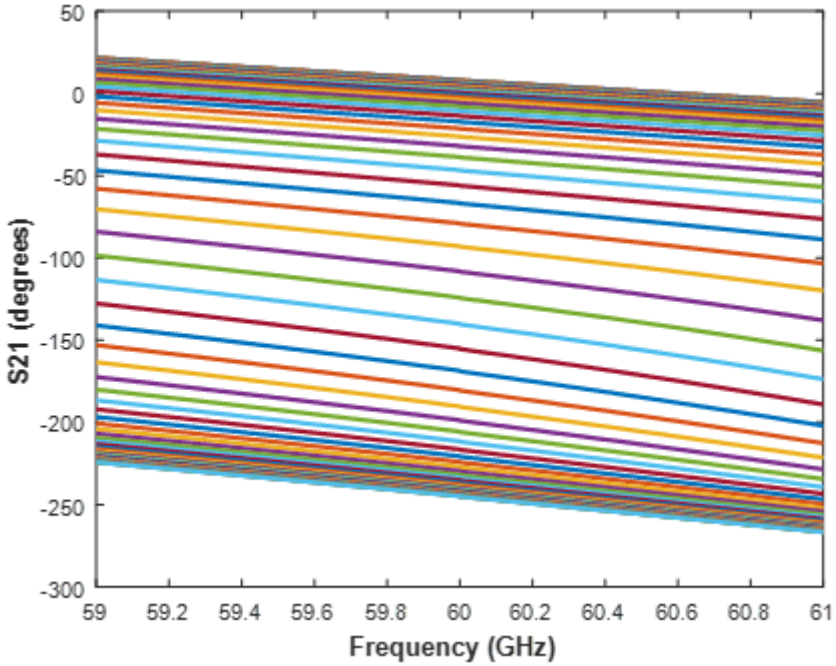


**Figure 7.45: Phase shift versus frequency of the overall phase shifter for various tuning voltages.**

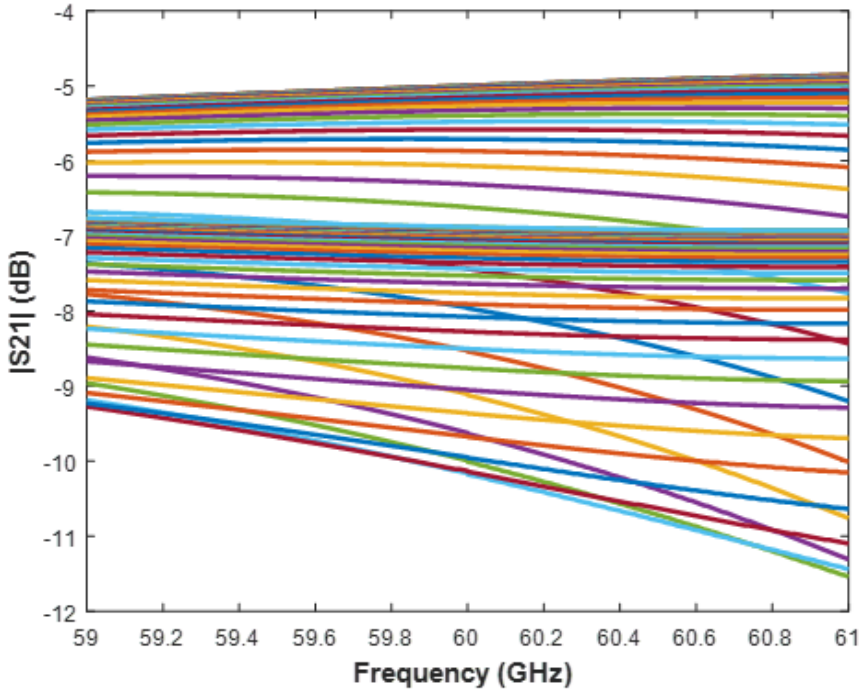


**Figure 7.46: Insertion loss versus frequency of the overall phase shifter for various tuning voltages.**

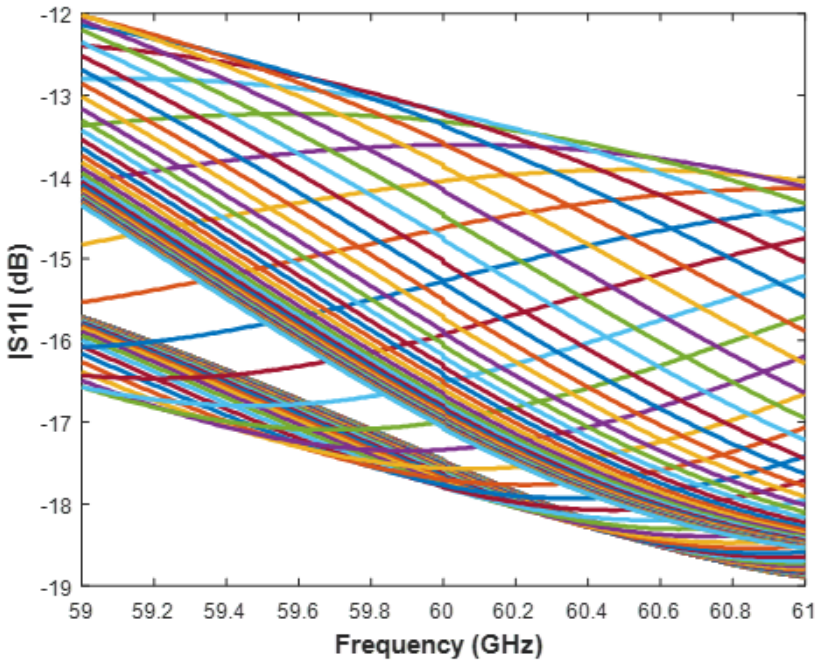


**Figure 7.47: Reflection coefficient $S_{11}$ versus frequency of the overall phase shifter for various tuning voltages.**

Figure 7.47 shows the RTPS reflection coefficient $S_{11}$ variation versus frequency, which is below -13 dB at 60 GHz across the tuning range, indicating good matching.

Figure 7.48 presents the RTPS reflection and transmission coefficients versus the control voltage, while Figure 7.49 presents the phase range variation across the tuning voltage where $\Delta\varphi = 254°$. Therefore, the RTPS achieves a high FOM of around 25°/dB.

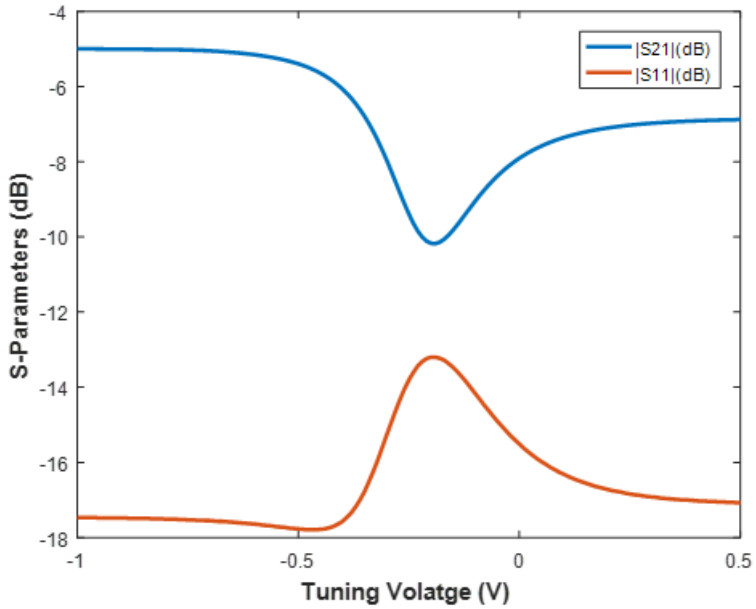


**Figure 7.48: Reflection coefficient $S_{11}$ and transmission coefficient $S_{21}$ (loss) versus control voltage of the overall phase shifter.**

All the steps for the IC design are performed on the RTPS, starting from DRC to LVS and ending with PEX, which are verified successfully.

Both Figure 7.50 and Figure 7.51 show the post-layout simulation of the RTPS in terms of its phase range, its insertion loss and its return loss. The FoM remains high but it is slightly reduced to reach around 22°/dB.

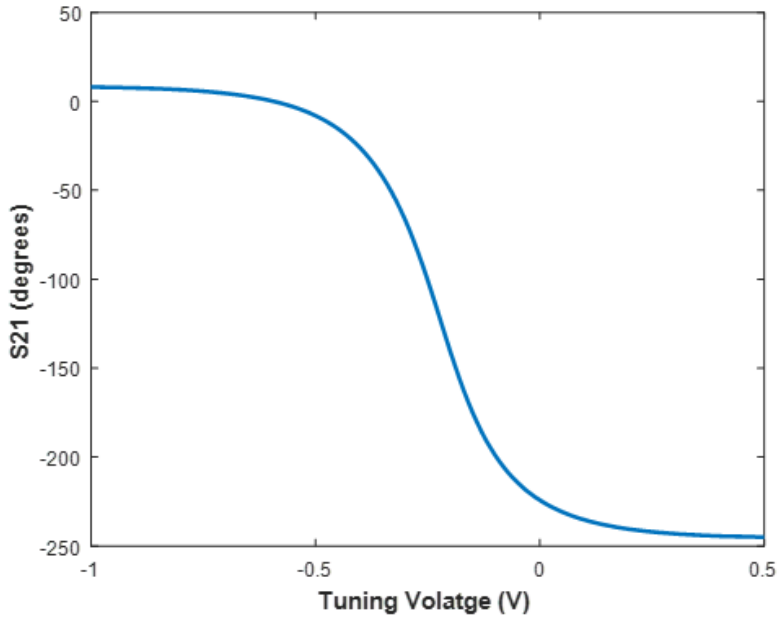


**Figure 7.49: Phase shift versus control voltage of the overall phase shifter.**

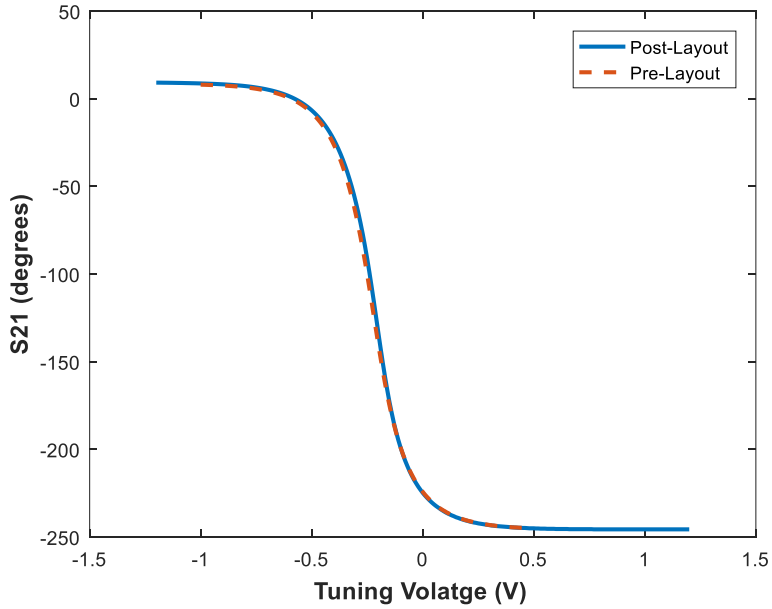


**Figure 7.50: Phase shift versus control voltage of the overall phase shifter for pre-layout and post-layout simulations.**

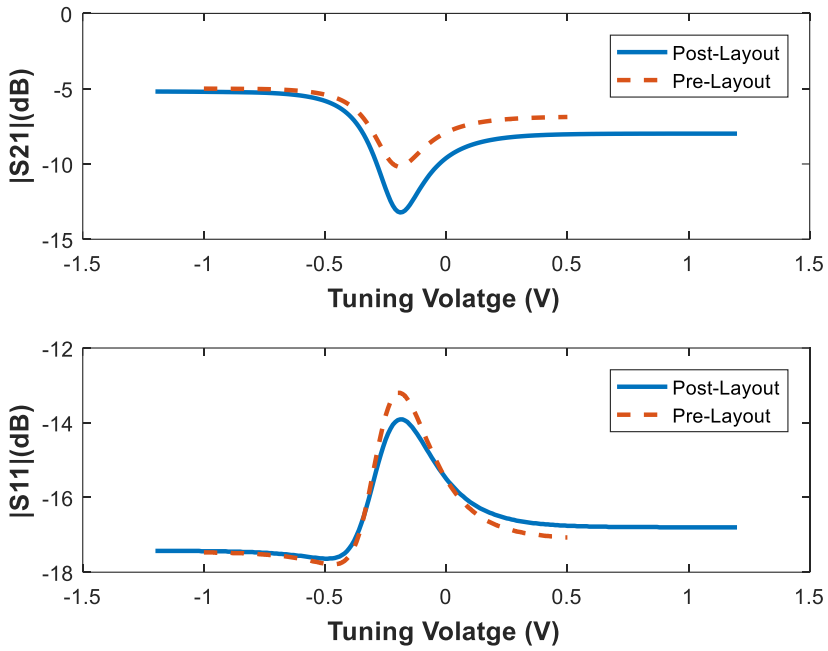


**Figure 7.51: Reflection coefficient $S_{11}$ and transmission coefficient $S_{21}$ (loss) versus control voltage of the overall phase shifter for pre-layout and post-layout simulations.**

Table 7.2 compares the performance of the work presented in this thesis (simulation results) to different RTPS designs implemented in silicon that have been fabricated and measured.

**Table 7.2: Performance Comparison of RTPS Designs Implemented in Silicon**

| Reflective Load | 4th order | Series L-C | $\pi$ network C-L-$C_{tuned}$ | Binary-weighted digitally-controlled varactor arrays (3-bit) | Transformer-based multi resonance |
|---|---|---|---|---|---|
| Coupler Implementation | Standard Hybrid | Broadside | Broadside | Transformer-type | Differential transformer-based |
| Core Area ($mm^2$) | 1.12 | 0.027 | 0.08 | 0.034 | 0.16 |
| Min Return Loss (dB) | 13.2 | 15 | 12 | 12 | 10.4 |
| FOM ($°/dB$)(1) | 25 | 17.6 | 11.25 | 13 | 37.1 |
| IL variation (dB) | 5 | 3 | 3.5 | 2.44 | 6.5(2)<br>0.7(3) |
| Max IL (dB) | 10.18 | 10.8 | 8 | 6.91 | 10.2(2)<br>10.3(3) |
| Phase Range | 254 | 190 | 90 | 90 | 367 |
| Freq (GHz) | 60 | 57-64 | 50-65 | 54-66 | 62 |
| Process | 90 nm CMOS | 90 nm CMOS | 90 nm CMOS | 65 nm CMOS | 130 nm BiCMOS |
| Ref | This work | [61] EuMC 14’ | [31, 62] MWCL 09’ | [32] MWCL 14’ | [60] TCAS-1 18’ |

(1) $FoM = \frac{\Delta\varphi_{max}}{IL_{max}}$

(2) Minimum IL settings

(3) Constant 10 dB IL circle settings

Note that the above FoM does not take into consideration the core area of the design.

## 7.7 Envisioned Measurement and Testing

It is well-known that the metrology of mm-wave modules is challenging due to the increase in measurement errors at these high frequencies. In order to characterize mm-wave designs, waveguide (WG) based measurement system is classically adopted, where the DUT is placed in a rectangular waveguide to be characterized. Despite the fact that it is time-consuming and cost-ineffective, one major advantage of this measurement setup is that only one single mode of propagation is present at the interface to the chip, where the cutoff frequencies of the lowest order and the next higher order mode of the waveguide dictate the useable frequency range. Such characteristic accurately assures what is being measured.

In order to overcome the limitations of the coaxial or waveguide transmission lines, RF probes are developed and act as adapters between the WG and the DUT pad interconnects. Such probes allow a direct measurement of the device performance without the need of prior packaging.

Figure 7.52 presents a photograph of a typical on-wafer RF probe based measurement with a close-up of its tip. Note that the probe tips show three signal conductors that are placed in a ground-signal-ground configuration, which connect both mechanically and electrically to the DUT.

On-wafer RF probe measurement system is prone to several parasitic effects as depicted in Figure 7.53 such as radiation, substrate coupling, and unwanted modes due to the multimode propagation unlike the single mode propagation offered by the WG based measurement setup. Another problem that arises is the cross coupling between input and output RF probe in the case of the RTPS. These problems increase the measurement errors, and this is worsened towards higher frequencies, especially that the RF probe

dimensions become large and comparable to the operating wavelength. One approach to mitigate the effect of these problems is to build accurate CAD models for EM field simulations for the RF probes used in the measurement setup as shown in Figure 7.54. Such approach also helps distinguish the effect of the RF probes to fabrication and process variations [63, 64].

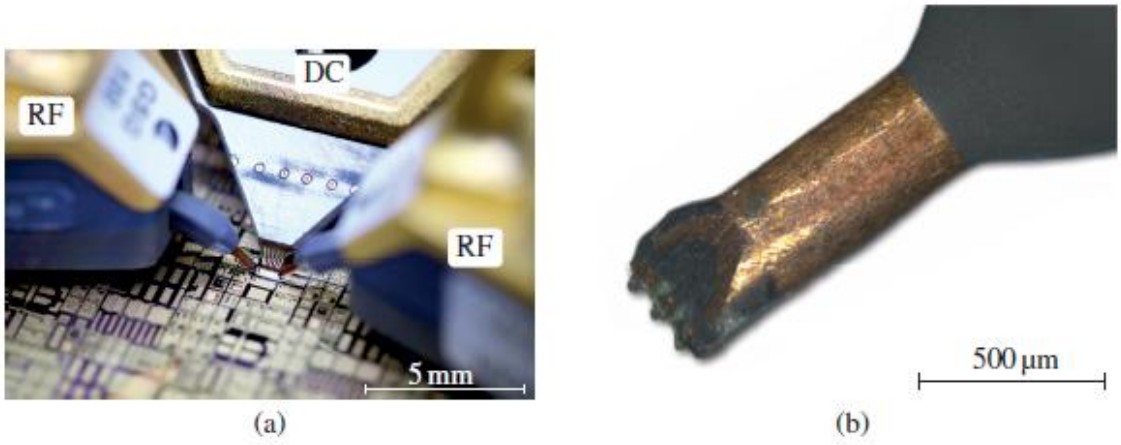


**Figure 7.52: Photograph of a (a) typical on-wafer RF probe based measurement and (b) close-up of a common RF probe tip [63].**

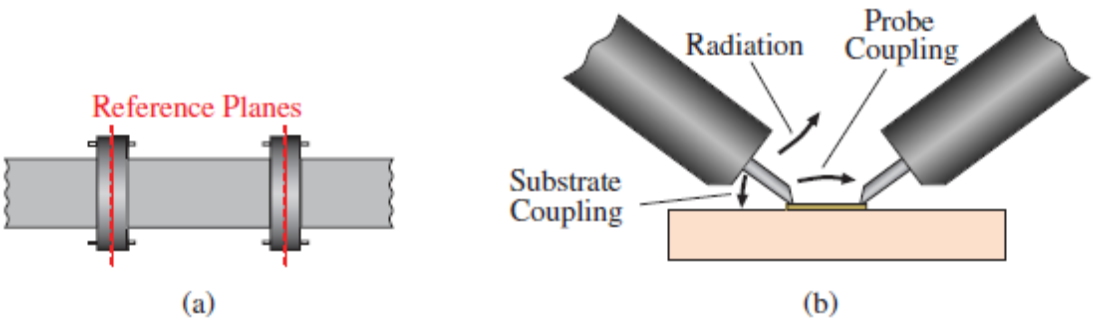


**Figure 7.53: Exemplary measurement of a simple line section for (a) WG based measurements and (b) RF probe based measurements [63].**

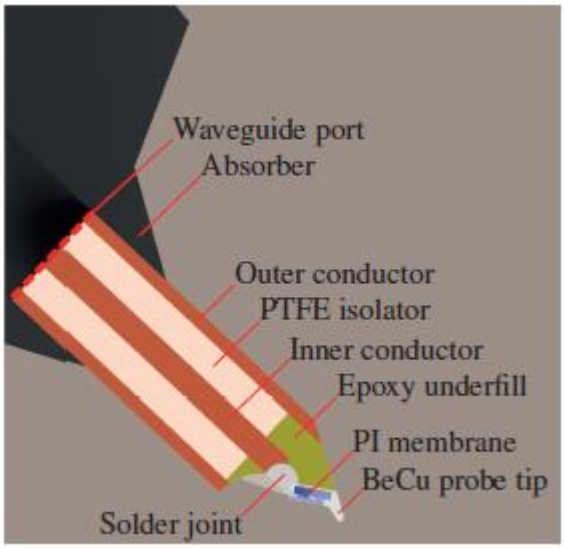


**Figure 7.54: Cross-section of the CAD RF probe models [63].**

## 7.8 Discussion

Featuring high linearity and low DC power consumption of ~ 25 $\mu$W, the newly proposed mm-wave RTPS is characterized by a reasonably low insertion loss and a maximum phase range of 254°, resulting in a high figure of merit of around 22°/dB. Its main drawback is the core area reaching around 1.12 mm$^2$. A possible improvement is by replacing the hybrid coupler by a broadside type or transformer-type coupler.

# CHAPTER 8

# CONCLUSION AND FUTURE WORK

In this thesis report, a new millimeter wave reflective-type phase shifter for phased array systems is presented. The phase shifter is one of the key blocks in the phased array feeding network design that enables beam steering capability. It is designed at 60 GHz and implemented in the 90 nm industrial CMOS technology. The design is achieved via co-simulations between Cadence Virtuoso platform and AED HFSS 3-D layout. A 3-dB hybrid coupler and two identical reflective loads terminating both the through and the coupled ports of the coupler are presented. The proposed $4^{th}$ order reflective load has a new asymmetric topology and employs two AMOS-based varactors and two inductors. Featuring high linearity low DC power consumption of ~ 25 $\mu$W, the passive reflective type phase shifter achieves a maximum phase range of 254° with a low insertion loss, resulting in a high figure of merit of around 22°/dB.

State-of-the-art phased arrays are presented in Chapter 2. Knowledge regards the ability to overcome key phased array design challenges is gained especially both at the mm-wave and terahertz frequencies. Novel beam steering approaches and feeding network designs with reduced complexity are discussed. These designs are shown to improve the scanning range and the array scalability respectively.

Common topologies of phase shifters are presented in terms of their pros and cons in Chapter 3. Despite its high insertion loss, RTPS is presented as a good candidate for the phased array feeding network due to its high linearity, its low DC power consumption as well as its simple control scheme.

MOS varactors as key components of RTPS in mm-wave RFIC design are discussed in Chapter 4. AMOS-based varactors are employed due to their high phase variation.

The knowledge of data acquisition and processing is acquired through the implementation of a software algorithm developed in order to extract the scattering parameters of back end circuitry as presented in Chapter 5**.**

The ability to design and test a phased array at microwave frequencies with its feeding network is attained as shown in Chapter 6. The radiation pattern of the implemented four-element linear phased array is shown to be steered to approximately 15° validating the beamsteering capability enabled by the phase shifters.

Moreover, expertise in analog/RF IC design is gained through the design of the proposed mm-wave RTPS as discussed in Chapter 7. 90 nm industrial CMOS technology design requirements as well as mm-wave challenges have been dealt with and met.

The research conducted in this thesis can be further extended by the following aspects:

- Miniaturizing the RTPS design, by for example replacing the hybrid coupler with either a broadside type or a transformer-type coupler.
- Exploring some additional types of phase shifters, such as active ones.
- Designing the remaining blocks of the feeding network as well as the antenna array at 60 GHz.
- Assembly, implementation, and testing of the standalone full phased array system.

- Building a software control for beam steering, which is able to extract the response of the millimeter wave phased antenna array as part of a complete device.

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