

AMERICAN UNIVERSITY OF BEIRUT

Ultra-low Power Wake-up Receivers for IoT
Devices with Application to Smart Agriculture

by

Ahmed Abed Benbuk

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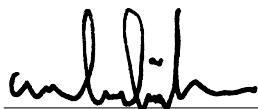
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An Abstract of the Thesis of

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Radio Frequency (RF) energy harvesting has been proposed as a solution to power the increasing number of Internet-of-Things (IoT) devices. Exploiting this energy source is challenging because RF signals attenuate quickly. Therefore, a solution must be found to minimize the power consumption of the numerous devices relying on harvested RF energy. RF wake-up is a mechanism that is employed to reduce the power consumption of IoT devices by switching them ON only when they are required to operate. This solution requires an RF wake-up receiver to process an external wake-up signal. Wake-up receivers have a strict power consumption requirement and, therefore, must maintain a simple architecture, while being able to detect a targeted wake-up signal.

In this work, we design an address detector for an RF wake-up receiver that uniquely identifies a sensor through an address that we encode in the detector's hardware. The proposed architecture is optimized for situations where an antenna is used for harvesting and wake-up. We propose a multi-power-state design to power the minimal components required to process a wake-up signal and minimize power consumption. We integrate our solution with a rectifier and Power Management Unit (PMU) to perform both RF harvesting and wake-up using the same antenna and rectifier. Further, we implement the system in an IoT smart agriculture application where wake-up signals are transmitted to control the operation of sensors using commercial routers. We study the efficacy of using UAVs as a transmitter to cover large agricultural fields. Our results show that implementing wake-up and harvesting can extend the lifetime of agricultural sensors which span large areas and communicate via wireless transceivers. Finally, we support our work with detailed experimental results and analysis.

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Chapter 1

Introduction

1.1 Project Background

An increasing number of devices are being connected to the internet realizing the concept of Internet of Things (IoT). Employing a large number of interconnected objects can be useful for different applications, including medical, agricultural, and industrial. However, the implementation of the IoT concept comes with multiple technical challenges. The long period of operation of these devices necessitate a solution for their power consumption [6] [7]. It is common to place IoT devices in a low-power (sleep) mode to prolong their battery life and operate them only when required. Furthermore, alternative methods have been explored to rely on ambient sources of energy in applications such as environmental monitoring where it is not easily feasible to replace the device's battery.

RF energy is seen by many as an attractive source for IoT applications due to the prevalence of wireless signals such as TV, radio, and Wi-Fi. Furthermore, RF harvesting circuits are characterized by a small size and a fair degree of complexity [8]. Nevertheless, taking advantage of this energy source comes with many challenges as it suffers from low power densities [9] [10], which requires the close deployment of energy sources to powered devices and significantly limits the harvesting range. In many applications, IoT devices operate for short periods and spend most of the time in an idle state. Therefore, one approach to reduce the energy waste is to set the main transceivers in a low power state along with the main circuitry, where the power consumption decreases significantly, and switch them to the active state only when required. This concept is known as RF wake-up, as it includes using a dedicated external circuit, an RF wake-up receiver that is used to trigger the main radio only when required, greatly reducing power consumption of the main device. Wake-up receivers must be always powered ON and therefore must have a minimal power consumption. On the other hand, they must be able to

efficiently detect the wake-up signal and avoid a false wake-up of the main device, which leads to wasted energy.

1.2 RF Wake-up Taxonomy

Systems that implement RF wake-up are typically comprised of a combination of the following components:

1. **RF Wake-up Transmitter:** The wake-up transmitter (WuTx) is the component that generates and transmits an RF wake-up signal to activate a specific (or multiple) IoT device(s).
2. **RF Wake-up Signal:** The wake-up signal (WuS) is transmitted by the wake-up transmitter and processed by the wake-up receiver. It contains a unique address if targeted wake-up is required.
3. **Wake-up address:** The unique pattern (sequence) that identifies a specific IoT device. This pattern is modulated by the wake-up transmitter into a wake-up signal. It is demodulated and processed by the wake-up receiver.
4. **RF Wake-up Receiver:** The wake-up receiver (WuRx) is the system that detects, demodulates, and processes a wake-up signal and generates a wake-up trigger to activate an IoT device. It includes the whole RF receiver chain (antenna, matching network, mixer, rectifier, amplifier and other components)
5. **Address Detector:** A component within the wake-up receiver that is responsible for correlating the demodulated wake-up signal. It generates a trigger if the IoT device's address is detected.
6. **Wake-up Delay:** The time required by the address detector to process a demodulated wake-up signal and generate a trigger.
7. **IoT Device (Unit):** This is the IoT device (sensor or actuator) that is targeted for activation from sleep mode into active mode. It operates on a limited power supply and spends the majority of the time in sleep mode.
8. **False Positives (False Wake-ups):** False activation of the the IoT device. This can either occur due to background noise detected by the wake-up receiver as a valid wake-up signal, or due to a wake-up signal that is intended to another IoT device but it is correlated with error.

9. **False Negatives:** Non-activation of an IoT device either due to background noise corrupting the wake-up signal or a wake-up signal that is intended to this IoT device but is correlated with error.

1.3 System Model



Figure 1.1: System Model

The system model is shown in Figure 1.1, where an IoT device receives RF charging and wake-up signals from an RF energy/wake-up transmitter. The IoT device remains in sleep mode, charging its battery, at the absence of a wake-up signal. When a wake-up signal containing the device’s address is received, the targeted device switches to the active state for a specific time in order to perform a task, and then it goes back to sleep mode. Noise signals, such as RF wake-up signals transmitted to other devices, or users in the network transmitting signals at the same frequency, can have a detrimental effect on the system’s performance by causing false wake-ups of IoT devices. Due to the fact that the system’s ambient noise cannot be controlled, the address detector should be designed in the target to minimize the probability of false wake-ups caused by noise.

In this work, we design a multi-power-mode address detector for combined RF wake-up and harvesting operations. The address detector uniquely identifies

a device through an address that we encode in its hardware, without the need for software-based processing. We integrate the address detector in a wake-up receiver that also accommodates an antenna and a rectifier circuit. The address is composed of a preamble, followed by a series of pulse-width modulated (PWM) modulated bits. The address detector switches between multiple states of power consumption to reduce its power consumption while processing the wake-up signal.

Furthermore, we design a power management system for harvesting the received RF signals and charging a storage element that can be used to power the address detector or an IoT device. The system is designed to satisfy the requirements of an IoT smart agriculture implementation. We integrate our work with a commercial wireless agriculture monitoring system and show that the RF wake-up mechanism reduces the sensor's power consumption. Furthermore, We exploit the high mobility of a UAV for wake-up and harvesting to extend the lifetime of numerous sensors implemented in agricultural fields.

The rest of this report is organized as follows: In Chapter 2, we conduct a literature review on recent developments of IoT in the field of agriculture. In addition, we review recent advancements in RF wake-up technology along with a discussion of different RF-based wake-up receiver designs. In Chapter 3, we provide a detailed system description and introduce the problem of combined RF harvesting and wake-up. Chapter 4 examines the design and implementation of an address detector architecture for combined RF harvesting and wake-up. In addition, Chapter 5 presents the Power Management Unit (PMU) design and implementation for passive RF energy harvesting. In Chapter 6, we provide analytical results to study the current consumption of the proposed address detector architecture under noise-free and noisy conditions. Chapter 7 presents an experimental study of using an Unmanned Aerial Vehicle (UAV) for combined RF harvesting and wake-up. Finally, we provide a conclusion and discuss future challenges in Chapter 8.

Chapter 2

Literature Review

The objective of this literature survey is to give a general overview about some important concepts related to the thesis work. We present IoT applications in agriculture. Then we review the state-of-the-art of wake-up receiver designs, and discuss the advantages and disadvantages of the proposed architectures.

2.1 A Review of IoT in Agriculture

The underlying technology of IoT makes it a suitable solution for realizing smart agriculture as it relies on sensor networks in different applications such as managing irrigation systems, applying fertilizers, greenhouse management, and pest control [11] [12] [13]. Many IoT deployments in agriculture have been proposed in the literature. An example is presented in [14] where the authors design a greenhouse system containing a collection of sensors for the optimization of plant growth. The system is implemented in a greenhouse with dimensions of $1.2 * 1.2 * 2.0 \text{ m}^3$ as shown in Figure 2.1. The proposed concept can be expanded into larger greenhouses, but this would require migrating to a wireless sensor network (WSN). As a result, batteries of sensors used such as DHT11 [15] would be quickly.

A wireless IoT irrigation system with scheduled wake-ups is provided in [16] employing wireless sensors to control soil moisture. The sensors trigger an ultra-low power microcontroller to transmit the measurements wirelessly via a Zigbee module. The Zigbee module and the microcontroller are put to sleep mode, and all sensors have scheduled wake-ups with no addressing capability. This leads to an average current consumption of 0.455 mAh (250 mA in active mode and 4.47 μA at sleep mode).

The author in [17] proposed an IoT long-term solution to detect wildfires. The system is composed of an NTC thermistor as an active device that is set in a voltage divider where the voltage across the thermistor changes with temperature.



Figure 2.1: IoT traceability system implemented in an experimental greenhouse in [1])

The microcontroller has a current consumption of $600 \mu\text{A}$ and each transmission requires a current consumption of 30 mA . By implementing a wake-up functionality, the thermistor can be triggered when the surrounding temperature exceeds a certain threshold during high risk seasons.

The increased average power consumption due to scheduled wake-ups is demonstrated in the designs proposed in [18] and [19]. In [18] the authors design a 802.11b/g battery-powered system that monitors environmental variables. All sensors are triggered simultaneously on a cycled schedule. The average current consumption is 25.68 mA when the device is turned on for 13 seconds and the sleep current is $10 \mu\text{A}$. This difference between active and sleep current consumption implies that the battery lifetime is greatly affected by the duty cycle. The average current consumption is around $587 \mu\text{A}$ for a duty cycle of 10 minutes.

The design in [2] demonstrates how scheduled wake-up greatly wastes energy that takes a long time to harvest and store. A microcontroller is connected in parallel with the storage capacitor. Charging the capacitor from 1.9 V to 3.75 V from ambient sources takes about 66 seconds. The microcontroller is programmed to wake up periodically every 60 seconds whether sensor data is required or not. This leads to draining all the harvested energy as can be seen in Figure 2.2.

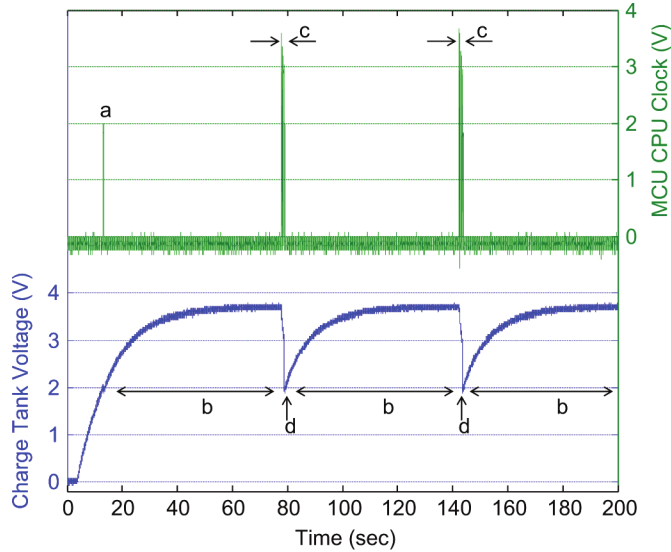


Figure 2.2: Harvested energy is discharged as the sensor is triggered periodically (Vyas et al. [2])

Scheduled operation of sensor nodes leads to overhearing and keeps the energy consumption high even at low wake-up frequency. For applications where the available power is low, there is a need for event-driven operation to wake-up the device only when it is needed. To provide that functionality, RF wake-up radios have been gaining considerable attention as they decrease power consumption by switching OFF the main circuitry, in addition to the possibility of providing selective wake-ups using addressing capabilities [20].

2.2 A Review of RF Wake-up Receiver Designs

The limited available power for RF wake-up receivers places a constraint on their sensitivity and complexity. Since the RF wake-up receiver is triggering the main radio, the entire system's sensitivity becomes that of the wake-up receiver. In their review in [21], the authors show that all low-power wake-up receivers with a power consumption under $10 \mu\text{W}$ implement ON-OFF keying (OOK) as the modulation scheme, as all other modulation schemes lead to a higher power consumption. The data rate is also a critical parameter for wake-up receivers. Wake-up signals with a longer duration keep the wake-up receiver active for extended periods, which increases power consumption. However, the longer transmission duration

also increases the range and reliability of the wake-up signal as it becomes more immune to interference [22]. Finally, the frequency of operation is an important factor because it determines the antenna's size. Higher frequency leads to smaller antennas; however, this also affects the range as signals with higher frequency decay faster.

Several technologies and standards are being implemented to realize the wake-up concept. For example, some designs are exploiting the pre-existing Wi-Fi infrastructure by designing wake-up receivers that operate at the 802.11 2.4 GHz ISM band. For example, the authors in [23] propose a wake-up receiver which uses an OOK modulation to emulate OFDM modulation used in the Wi-Fi standard. Other designs [3] propose wake-up receivers at the 868 MHz ISM band to extend the communications range. On the other hand, some designs are optimized for operation with the new 802.11ba standard which defines radios for extreme low-power operation with a power consumption of less than 1 mW [24].

Wake-up receivers can generally be classified by four distinct features: power source, addressing capability, channel usage, and medium [20]. Passive RF wake-up circuits do not require a continuous power supply, and they rely on harvested energy or the wake-up signal itself to power up. This burdens the transmitter that must transmit a wake-up signal long enough (typically few seconds) for the wake-up receiver to gather sufficient energy to operate, and therefore, delays the wake-up process [20]. The majority of current designs are active and semi-active wake-up receivers, characterized by higher sensitivity and addressing capability.

An example of a passive RFID wake-up system is proposed by the authors in [25]. An Intel WISP RFID tag [26] is combined with a Tmote Sky [27]. The WISP tag acts as a regular RFID tag that can be read by conventional RFID readers. However, it comprises a full RF energy harvester, which powers up the WISP, sensors, and a microcontroller. The activation distance is 4 meters with a transmitted power of 36 dBm. The wake-up range is later increased to 5.18 meters by adding a harvester composed of a 10-stage Dickson voltage multiplier.

To increase the sensitivity of RF wake-up receivers and maintain an addressing capability, active and semi-active approaches were considered in the literature. Thus, different techniques are presented to reduce their current consumption. Figure 2.3 shows a generic architecture and components of the wake-up receiver chain. The available efforts target one or more components to enhance performance and minimize current consumption. For example, the power consumption of the WuRx in [28] is reduced by 29% by lowering the Low-Noise Amplifier (LNA) gain during listening. An alternative method is presented in [29] where energy savings are achieved by relying on passive, lumped-element phase shifters to perform mixing. On the other hand, the work in [30] uses a passive, high-Q transformer/filter to achieve a passive gain of 25 dB.

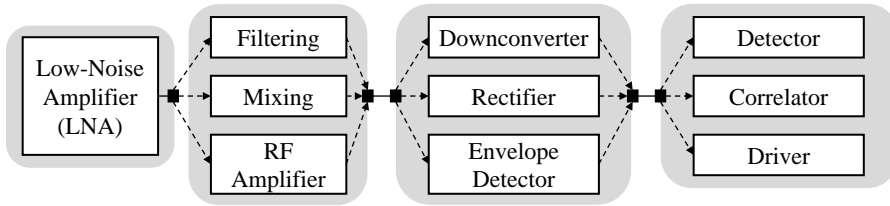


Figure 2.3: Generic structure of RF wake-up receivers presented in the literature

Different approaches are proposed in the literature to reduce the power consumption of the final stage of the receiver chain, which is typically composed of a baseband address detector that connects to an IoT device at its output. A conventional baseband architecture is shown in Figure 2.4. The received signal is demodulated by an envelope detector, and a data slicer converts the voltage signal into digital pulses. A correlator examines the serial bit sequence and produces a trigger when a match occurs. The correlator is either permanently powered on [31, 30, 32, 33, 24, 34, 35, 36, 37], duty-cycled [38], or placed in a low power consumption mode [23, 3, 39, 40, 41, 42] while in the listening state. Additionally, a local oscillator generates the clock required for synchronization [31, 38, 23, 30, 32, 33, 24, 35, 37].

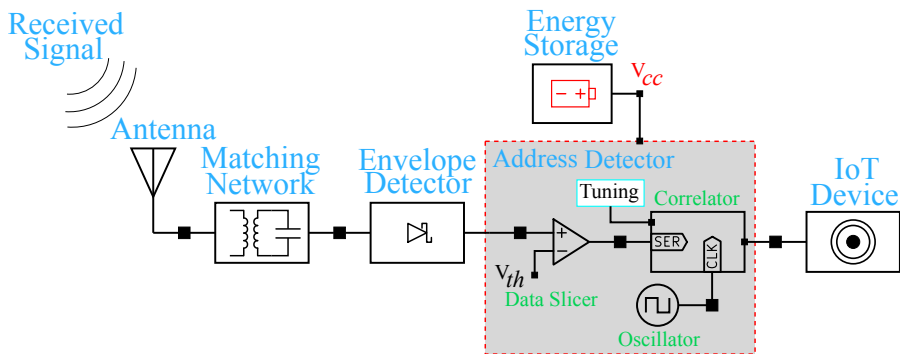


Figure 2.4: Conventional WuRx baseband architecture

The designs in [3] and [43] follow a similar architecture by relying on a micro-controller to process the address. Active components such as a DC-DC boost or comparators are used to increase the sensitivity. In [3] Magno et al. design a wake-up receiver (Figure 2.5) that starts with an antenna followed by an LC matching network operating at the frequency of 868 MHz. The received signal is rectified using a passive rectifier that employs Schottky diodes with a sensitivity of -57 dBm. A comparator with a sensitivity of -32 dBm and power consumption of 152 nW

interrupts the microcontroller. The comparator's output is connected to a passive noise-cancelling preamble detector to avoid false power-up of the microcontroller.

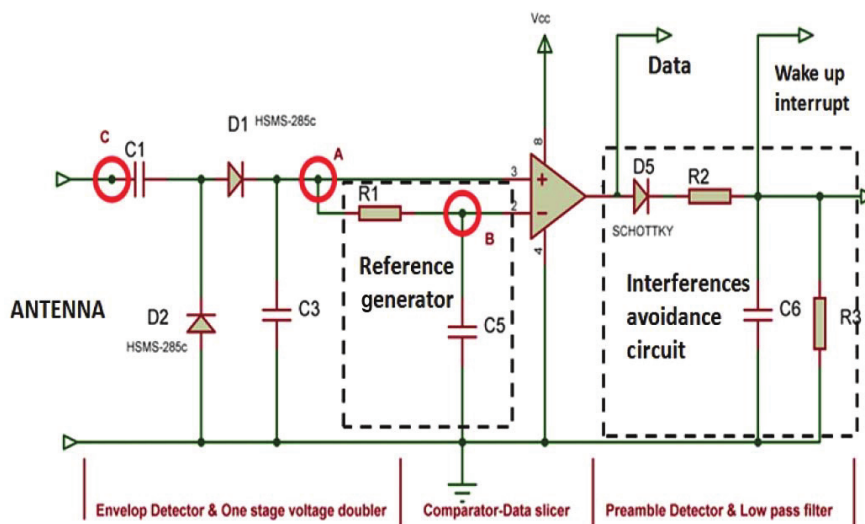


Figure 2.5: Wake-up receiver designed by Magno et al. [3]

Some designs [44, 45] rely on the commercial AS3932 IC [46] which can be used as an envelope detector at frequencies between 15 – 150 KHz as well as an address detector. These functionalities are achieved with a current consumption of $8.3 \mu\text{A}$ and a sensitivity of $80 \mu\text{V}$. In [47], the authors propose a wake-up receiver with an address encoded using sub-carrier modulation. The 868 MHz signal is demodulated to generate a 125 KHz signal for the AS3932. The authors report a sensitivity of -53 dBm ($80 \mu\text{V}$). In [45] and [44] the authors use the AS3932 to design a wake-up receiver at the 802.11 2.4 GHz ISM band. It has a sleep mode power consumption of $10.8 \mu\text{W}$ and $24 \mu\text{W}$ during address decoding and a wake-up range of 50 meters.

In contrast to relying on commercially-available components, some designs implement dedicated hardware for address decoding. In [33], a full wake-up receiver is designed and evaluated for operation at 802.11 2.4 GHz band. The wake-up receiver relies on D-flip-flops to process an OOK-modulated 16-bit address. The power consumption of the address decoder is $25.5 \mu\text{W}$.

In [41] the authors propose a wake-up receiver capable of functioning as an SPI master and demodulate PWM-modulated signal. The design is shown in Figure 2.6 and it includes a preamble detector that wakes up the microcontroller whenever a

preamble with a frequency exceeding 5 KHz is received. Following the preamble is a PWM-modulated signal which is detected using an RC circuit. The microcontroller switches only to Low-Power Mode-3 (LPM3) for SPI communication consuming a current of 1.8 μA .

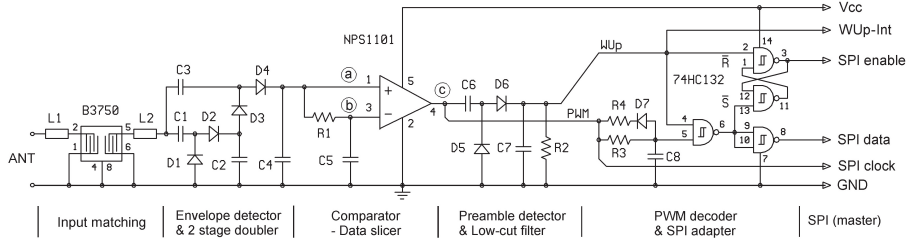


Figure 2.6: Wake-up receiver as an SPI master (Marinkovic et al.)

CMOS technology allows the design of complex wake-up receivers with a small size and low power consumption [28, 23, 30]. In [28] a wake-up receiver is designed with two operating modes where the gain of the RF amplifier is reduced during listening. It is followed by an envelope detector composed of a clock, shift registers, and several logic gates. This wake-up receiver is fabricated using a 130 nm process with a core size 0.2 mm² and achieves a sensitivity of -78.5 dBm and -75 dBm with a power dissipation of 16.4 μW and 22.9 μW when monitoring and processing an address, respectively. An alternative design is proposed in [23] where the authors develop a wake-up receiver based on an On-Off keying (OOK) emulating orthogonal frequency division multiplexing (OFDM) modulation scheme. The wake-up receiver is characterized by a power consumption of 95 μW and sensitivity of -72 dBm.

Chapter 3

Problem Definition and Thesis Objectives

Figure 3.1 shows the block diagram of a typical IoT wireless device containing different sensors. Introducing combined RF energy harvesting and wake-up offers reduced energy consumption of the microcontroller, transceiver, and sensors by keeping them in sleep mode (or shutdown) unless they are required to operate. An RF signal is received via a high gain antenna and converted into DC voltage. The antenna is followed by a matching network that ensures maximum power transfer to the rectifier, acting as an envelope detector that follows the incoming AC signal's peak. The rectified voltage is stored in an energy storage device.

The same DC output of the rectifier encodes a wake-up signal that is processed by the wake-up system. The rectifier acts as a passive demodulator from the receiving perspective. Its output is processed by the wake-up system to decide whether to wake-up the main components. The wake-up system can have a sleep mode to reduce its power consumption [3, 41].

The concept of combined RF harvesting and wake-up offers IoT devices enhanced autonomy by relying on the harvested energy to operate only when required (a wake-up signal is received). This concept is demonstrated in Figure 3.1, where the output of the rectifier diverges into the power storage unit and the wake-up system. Combining harvesting and wake-up operations leads to challenging design considerations. The combination of the two functions can adversely affect performance due to loading the receiver [48]. For most RF energy harvesters, the DC output is limited in amplitude, as well as their ability to act as a current source to drive the components existing in the wake-up receiver. Moreover, the RF wake-up circuit appears as an arbitrary load for the rectifier, which might also change its value if the wake-up circuit has multiple operational power modes. This requires co-designing the rectifier and the wake-up receiver to ensure compatibility between the two systems and reduce energy drain.

The harvested energy is seen as a noise signal by the wake-up receiver, and can cause false wake-ups if it is decoded as a wake-up signal. This problem is exacerbated by the wake-up system’s limited processing capabilities, especially when operating in sleep mode. For example, the added noise can activate the bit correlator from low power mode [3, 41] or cause a false wake-up of the IoT device [39] even when an interference-avoidance preamble detector is employed [3, 41]. We can demonstrate the false wake-up problem by considering the design in [3] shown in Figure 2.5. Particularly, we consider a PMU connected at the output of the envelope detector and one stage voltage doubler, in parallel with the address detector. The RF charging signal is a continuous DC voltage at point (A), causing the comparator’s output to turn HIGH. This leads to charging the RC circuit of R_2 and C_6 and interrupting the microcontroller, which attempts to decode the received ”address.” From Figure 2.2, we can see that such a behavior quickly drains a typical storage capacitor as the microcontroller treats the harvested signal as a received wake-up signal by switching from sleep to active mode.

Recently, the coded preamble concept has been considered as a potential strategy to enhance wake-up signals’ data delivery efficiency and improve interference avoidance [49]. The existing efforts exploit the preamble for the sole purpose of interference avoidance [23, 41] or synchronization [38, 23, 24, 50, 28], but do not consider the preamble’s potential for carrying specific instructions. In addition, various methods have been implemented to eliminate dedicated oscillators for clocking [51, 52, 53].

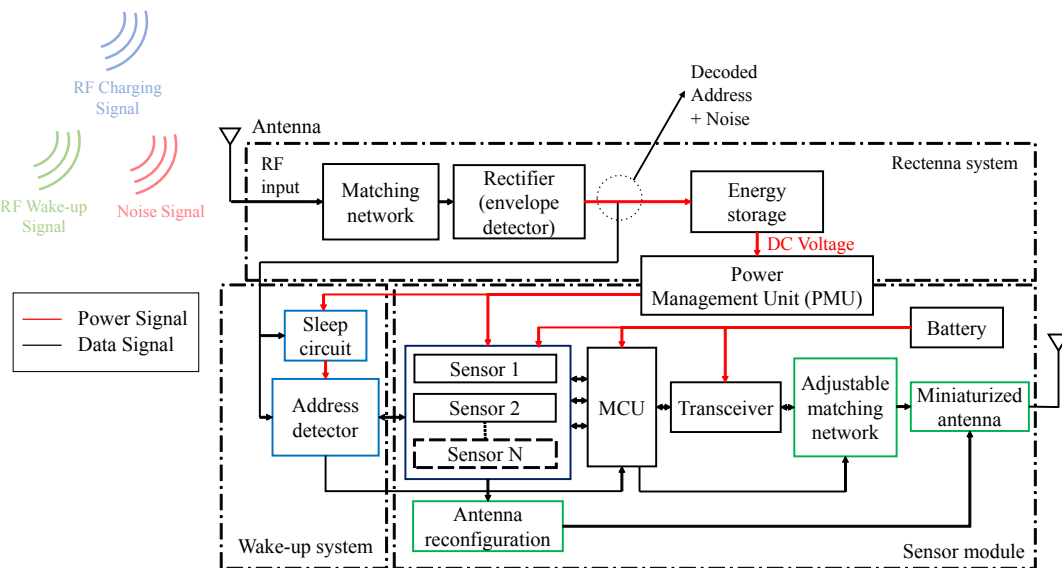


Figure 3.1: Combined RF harvesting and wake-up

Based on the above, the objectives of this thesis can be summarized as follows:

- Design, implement, and test a novel baseband architecture for combined RF charging and wake-up using an ultra-low-power multi-power-mode address detector for decoding a wake-up signal composed of a coded preamble and a PWM-modulated bit sequence.
- Employ a coded preamble detector embedded in the address detector that enhances data delivery efficiency and immunity against interference. The coded preamble precedes the bit sequence and can be used to extend the addressing range, or implement advanced techniques, such as multicast addressing capability [54]. We Realize an asynchronous solution by extracting the bit correlator’s clock from the input bit sequence, removing the need for a local oscillator and bit oversampling that is implemented in the majority of designs in the literature.
- Design a Power Management Circuit (PMU) to store the harvested energy and power the wake-up receiver. The PMU must appear as an appropriate load looking fro the rectifier and in parallel with the address detector.
- Integrate and test the designed wake-up receiver and the RF energy harvester with an agricultural monitoring solution to demonstrate real-world applicability and evaluate the benefits of dedicated wake-up for prolonging the lifetime of agricultural sensors
- Provide an analysis of the performance and capabilities of an IoT agriculture solution to confirm the benefits of RF wake-up in realizing smart agriculture.

The goals and requirements of the obtained solution are shown in Table 3.1:

Table 3.1: Requirements of the Combined RF Harvesting and Wake-up System

| Aspect | Requirement |
|-----------------------------------|--------------------|
| Frequency | 2.4 GHz |
| Sensitivity (Wake-up) | < - 30 dBm |
| Sensitivity (Harvesting) | < - 15 dBm |
| Address Range | 2^8 |
| Consumption (Active) | < 10 μ W |
| Consumption (Sleep) | < 1 μ W |
| # of Antennas and Rectifiers/Unit | 1 |

Chapter 4

Address Detector Design

This chapter discusses the main objective of this work, which is the design and implementation of an ultra-low-power address detector for wake-up receivers. We aim to achieve the following goals:

1. Maintain a simple architecture and low cost per unit
2. Operate on a minimal current consumption to maximize lifetime
3. Tune the address detector to different addresses without making a drastic change to the architecture
4. Maximize the size of the address range

Wake-up receivers must maintain a simple architecture to reduce cost and current consumption. Meanwhile, the design should be scalable to address a large number of potential IoT units. We will avoid the use of a microcontroller or software processing, and obtain an asynchronous design, unlike most other works in the literature [3, 44, 41, 23] to reduce energy consumption and avoid synchronization-related issues.

As shown in Figure 4.1, the address detector is placed at the output of a rectifier and its input is a modulated baseband signal. Using a rectifier as an envelope detector offers the advantage of passive demodulation, in contrast to the heterodyne architecture [20] which uses active mixing to down-convert the RF signal. Under these concerns, we consider the different possible modulation schemes of the RF signal at the output of the rectifier, shown in Table 4.1. Frequency- and Phase-based modulated RF signals cannot be demodulated using a rectifier, hence these schemes are not considered in this work. Amplitude-shift modulation of the RF signal cannot be considered because the amplitude of the baseband signal is a function of the amplitude of the modulated RF signal and

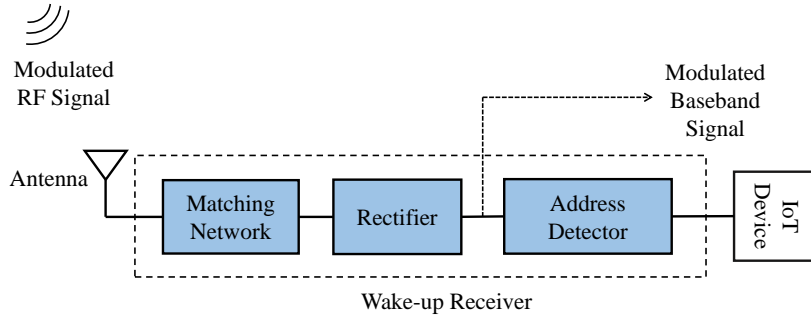


Figure 4.1: Block diagram of the wake-up receiver showing RF and baseband modulated signals

the rectifier’s non-linear response [55]. On the other hand, the OOK and PWM modulations can be used with a variety of standards. For example, a Wi-Fi channel can be specified for wake-up operations by modulating the carrier to encode an address. Furthermore, the baseband can be used in wake-up receivers operating within the 802.11ba standard which uses multi-carrier (MC-OOK) for extremely low power communications. Based on these considerations, we adopt OOK and OOK/PWM as the modulation schemes for the RF signal. In the OOK modulation scheme, the RF signal has two distinct states. In the OOK/PWM modulation scheme, additional information is encoded in the signal’s period (width).

Table 4.1: Possible Modulation Schemes at the Output of the Rectifier

| RF Signal Modulation Scheme | Demodulated Baseband Signal |
|------------------------------|-------------------------------|
| OOK-modulated RF carrier | OOK-modulated baseband signal |
| OOK/PWM-modulated RF carrier | PWM-modulated baseband signal |
| ASK-modulated RF carrier | ASK-modulated baseband signal |
| FSK-modulated RF signal | NA |
| PSK-modulated RF signal | NA |

4.1 Pulse Width Detector Design

By considering the available modulation schemes highlighted in Table 4.1, the simplest baseband modulation is a pulse with a variable width where the width of

the pulse encodes a unique address. The authors in [56] propose a similar concept, described as frame length modulation. The idea of encoding a unique address in the pulse width is presented in Figure 4.2. A wake-up transmitter generates a wake-up signal that is received by two wake-up receivers tuned to two different addresses. The bottom of the figure shows the baseband signal (modulated pulse) used to target a specific IoT device. The two wake-up receivers are identical except for their address detectors, tuned to detect different addresses encoded in the pulse width (T_D). This approach suffers from scalability issues because the wake-up delay increases with the number of addresses. For example, wake-up receiver 1 has a larger wake-up delay when compared to wake-up receiver 2. Nevertheless, we consider this scheme because it is the simplest way to convey a unique detectable signal, and it does not require clocking at the wake-up receiver.

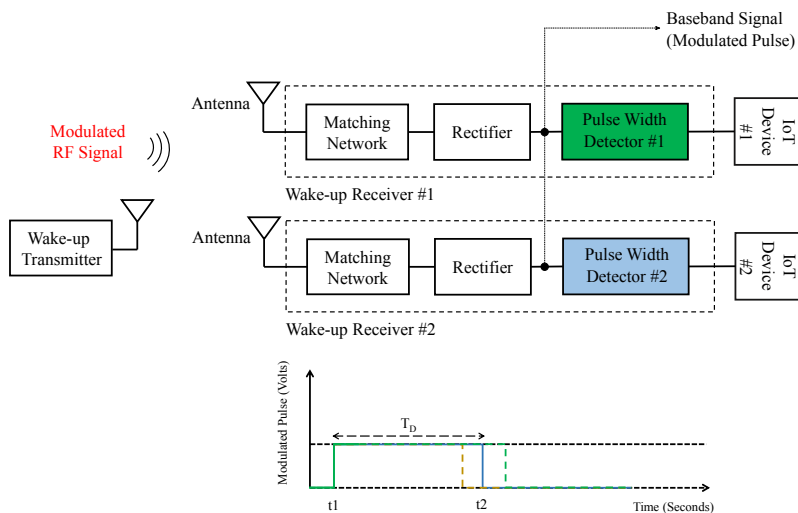


Figure 4.2: Encoding an address in the period of the ON state at the output of the rectifier

To decode the demodulated pulse width, we propose an ultra-low-power pulse width detector (PWD) [57] that is designed and implemented within an RF wake-up receiver (WuRx) operating at Wi-Fi 802.11b/g 2.4 GHz bands. The detector circuit relies on ultra-low-power components to achieve a selective wake-up without using a microcontroller for bit correlation. A block diagram of the designed circuit is shown in Figure 4.3. it is composed of two parts: a passive front end for detection and an active network for storage and trigger generation. The active storage is powered OFF when no wake-up signal is received i.e, when no voltage is detected at the rectifier's output.

The circuit implementation of the PWD is shown in Figure 4.4. The passive

front end is composed of two identical RC networks. The value of a variable resistor sets the upper and lower tuned pulse width limits. Each RC circuit is preceded by a Skyworks SMS3922 Schottky diode [58] which blocks the capacitor from discharging in the opposite direction. Capacitors C_1 and C_2 are charged through variable resistors R_1 and R_2 obtaining a charging time constant of $\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$, respectively. When the input is removed, the RC networks discharge through the shunt resistors which have an equal value of R_3 . By setting $R_2 > R_1$ the voltage level V_2 on the R_1C_1 network will always be higher than V_1 on the R_1C_1 network for any applied pulse width. The two voltage levels are compared after the pulse is fully received, and the width can be found.

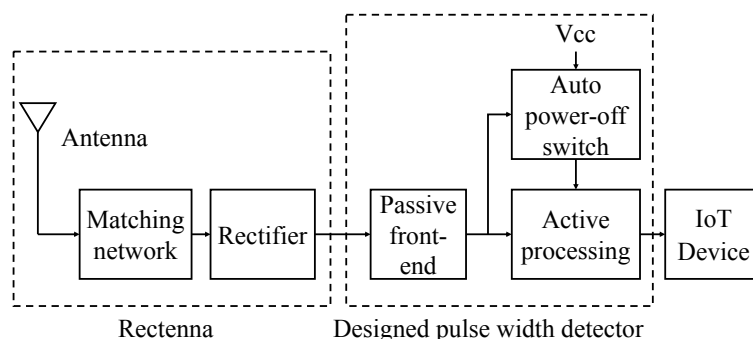


Figure 4.3: Block diagram of the designed ultra-low-power pulse width detector within a wake-up receiver

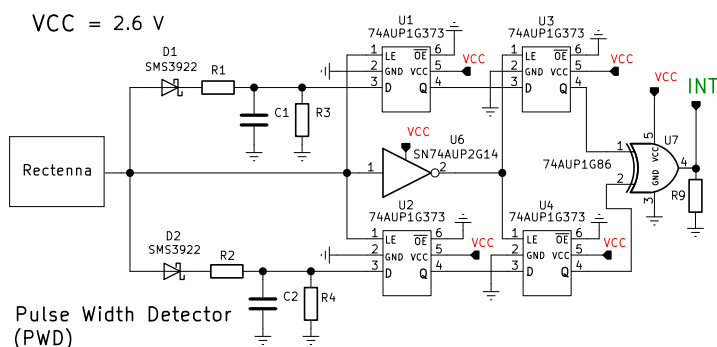


Figure 4.4: Pulse width detector circuit

Figure 4.5 shows the digital waveform of Case 2 and Case 3. The threshold

of the D-latches was found to be $V_H = 1.2$ V and $V_L = 1.04$ V @ $V_{CC} = 1.8$ V. For any input pulse with a width t we can differentiate three possible cases for the voltage levels V_1 and V_2

Case 1: $V_1 < V_{TH}$ and $V_2 < V_{TH}$ for $t < t_d \Rightarrow$ Output = LOW

Case 2: $V_1 > V_{TH}$ and $V_2 < V_{TH}$ for $t = t_d \Rightarrow$ Output = HIGH

Case 3: $V_1 > V_{TH}$ and $V_2 > V_{TH}$ for $t > t_d \Rightarrow$ Output = LOW

Where V_{TH} is the CMOS threshold of the logic gates in the active processing part and t_d is the tuned pulse width, in seconds. The previous cases correspond to the truth table of an XoR gate. However, for Case 3, the two RC networks remain below the threshold of the XoR gate (1.2 V @ 1.8 V_{CC}) simultaneously because their time constants are different. A network composed of Low-power D-latch gates [59] is used to hold the values of V_1 and V_2 until the pulse is fully received. The input signal sets the EN pins of latches D_1 and D_2 HIGH and enables writing new values in the D-latches. When the input is removed, the values of V_1 and V_2 appear at Q_1 and Q_2 as either a HIGH or LOW CMOS logic values. The output of D_1 and D_2 is directly connected to D_3 and D_4 . However, these two D-latches are enabled through an inverter [60]. The output of this D-latch network is directly connected to an XoR gate. [61].

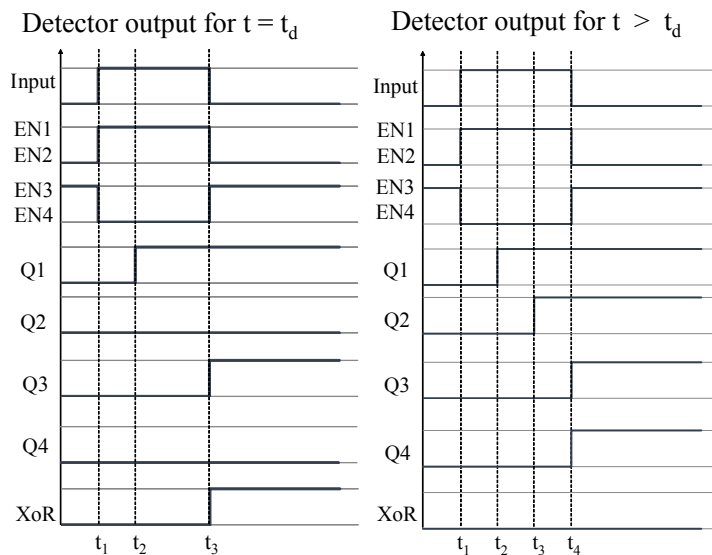


Figure 4.5: Digital waveform of the detector circuit

4.1.1 Pulse Width Detector Fabrication and Testing

The designed circuit is fabricated on a PCB with dimensions of $3 \times 2.5 \text{ cm}^2$ and is shown in Figure 4.6. The values of the passive front control the tuned address. R_1 and R_2 are set to $46.2 \text{ k}\Omega$ and $56 \text{ k}\Omega$, respectively. C_1 and C_2 are equal and have a value of $10 \text{ }\mu\text{F}$. R_3 is set to $330 \text{ k}\Omega$ for both RC networks to obtain a considerably larger discharge rate.

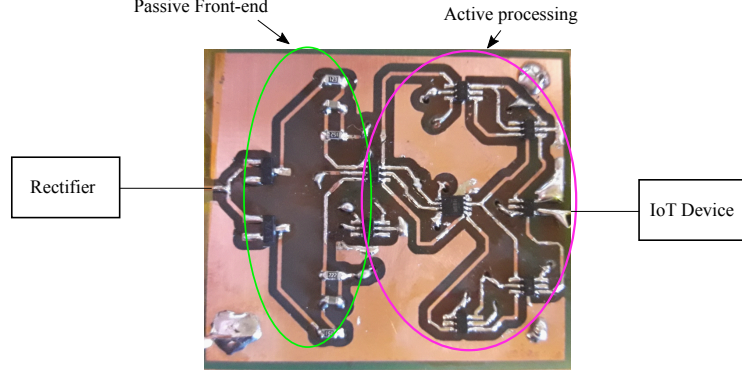


Figure 4.6: Fabricated pulse width detector circuit

The values of R_1 and R_2 are selected with minimal separation such that the output of D_1 is HIGH ($V_1 = 1.2 \text{ V}$) and the output of D_2 is low ($V_2 = 1.04 \text{ V}$) for an input pulse width of 800 ms . The experiment is repeated 10 times, and the values of Q_1 and Q_2 are recorded. The value of R_1 is increased to the maximum value at which the output remains HIGH when an 800 ms pulse is received. R_2 is tuned similarly by decreasing its value to the minimum value at which the output was LOW. The resistors' values were considered unreliable if at least one wrong output is obtained during ten attempts. When the values of V_1 and V_2 are between 1.04 and 1.4 V , the output is undetermined, causing false negatives or false positives.

The PWD can be tuned to different values of pulse widths ranging from the microsecond to the millisecond range. To demonstrate the PWD's flexibility, we tune the RC circuits to the values shown in Figure 4.7 to generate a trigger when a pulse width of $100 \text{ }\mu\text{s}$ is received. The input width is demodulated into the voltages recorded on the input of d-latches D_1 and D_2 , and the PWD generates a trigger. The active components do not need to be reconfigured for tuning.

Two RC circuits must maintain the relationship of $\tau_2 = 1.21\tau_1$ to generate an expected output. This leads to an exponential increase in the tuned pulse width when the number of IoT devices to be addressed with different pulse widths increases. The obtained experimental values were plotted against the theoretical ones to capture this increase. As shown in Figure 4.8, the tuned pulse width

increases exponentially when the number of required addresses increases, which limits the applicability of this addressing scheme for a large number of devices.

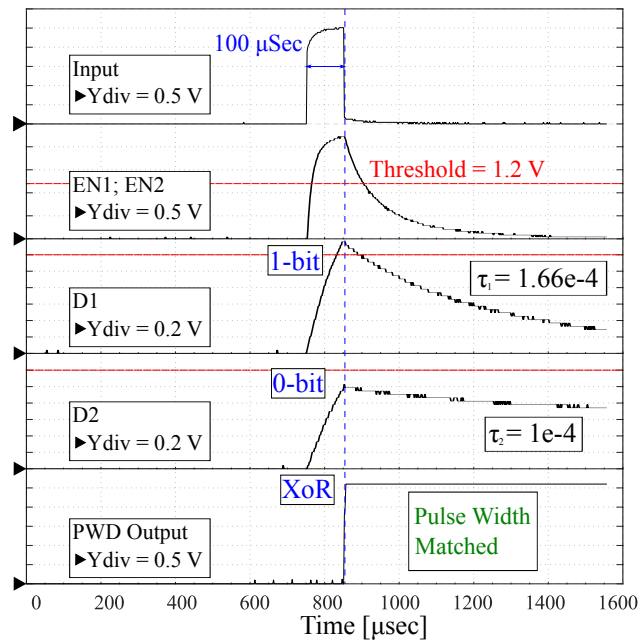


Figure 4.7: PWD operation. Pulse width detection is performed by varying the values of the resistors.

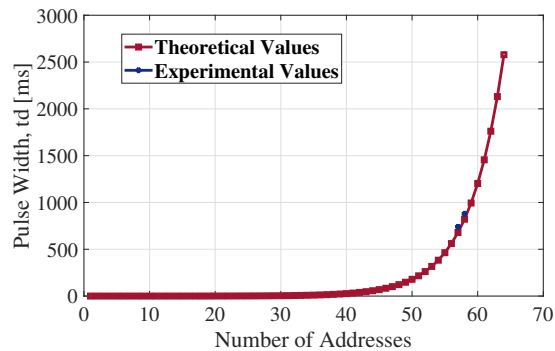


Figure 4.8: Pulse width t_d vs. number of addresses

The PWD is integrated with a load-independent tapered rectifier [55] and a high-gain antenna to obtain a wake-up receiver. The applicability of pulse width modulation as an addressing scheme is tested when the pulsed wake-up signal is

generated by the rectifier. Because the rectifier in [55] is load-independent, it can drive the pulse detector circuit without the need for a matching circuit. The responsiveness of the rectifier to the changes in the input power (rise/fall time of the rectifier’s output DC voltage) is found and compared to a dedicated signal. The slower change in the rise time makes the received pulse width appear shorter for the PWD. Different rectifiers have different responsiveness, and a comparison in [39] shows that the Dickson voltage multiplier [62] achieves the fastest response.

The error caused by the response time of the rectifier is evaluated using the setup shown in Figure 4.9. The PWD is tuned to different decreasing pulse widths received from a dedicated signal generator. This response is later compared to that received from a rectifier. The change in the rectifier’s output is slow, which causes more severe corruption for shorter pulses at the rectifier’s output.

The error value between the width of the input RF pulsed signal and the width of the demodulated signal at the output was found using:

$$Error\% = \frac{t - t_d}{t} * 100 \quad (4.1)$$

The results show that the decoding error limits the minimum pulse width that can be detected by the system, and sets a bottleneck on its highest data rate for PWM modulation of 1- and 0-bits. The smallest pulse width that is demodulated with minimum error is about 250 ms.

The PWD is tested within a wake-up system composed of a wake-up transmitter and receiver. The rectifier in [63] is connected to the output of a 2 x 1 meandered array operating at 2.24 GHz with a gain of 12.6 dB. The rectenna was first tested as a standalone receiving unit. A DC voltage of 1.8 V is obtained at the output of the rectifier for an input power of 0 dBm, as shown in Figure 4.10. The full system setup is shown in Figure 4.11 where the distance between the wake-up transmitter (WuTx) and WuRx is set to 50 cm. The received power at the rectenna is -1.9 dBm, and we obtain a DC output of 1.8 V. The WuTx emits a signal at $f = 2.42$ GHz for a period equal to $t_d = 800$ to 880 ms. The experimental results show that the WuRx is triggered for the input of that width range. Furthermore, the output of the WuRx remains LOW for $t_d < 800$ ms or $t_d > 880$ ms.

The average current consumption of the wake-up receiver is composed of two contributions. Namely, current consumption in active mode (when the wake-up receiver is processing a wake-up signal), and the current consumption in sleep

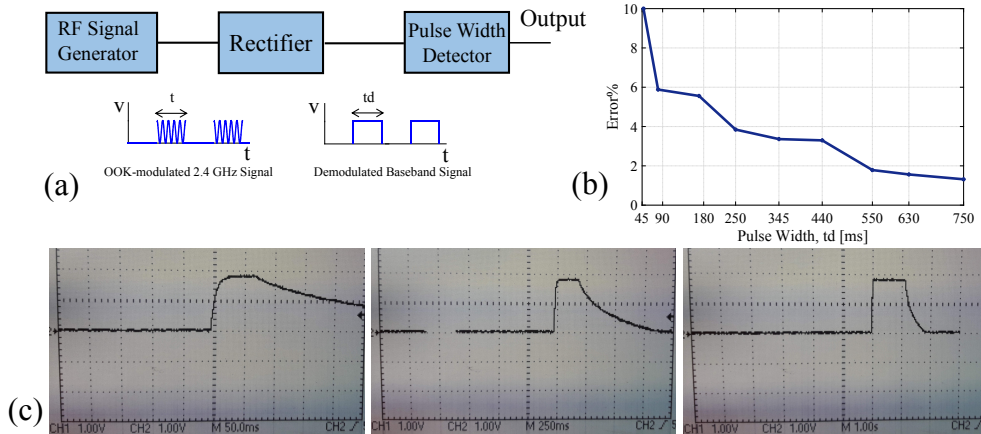


Figure 4.9: Testing the rectifier's response time. (a) An RF signal is generated for period t and driven into the rectifier. The width of the rectifier's output t_d is measured using an oscilloscope. (b) The difference in width between the input and output is calculated to find the error caused by the slow response of the rectifier. (c) Snapshots showing the output of the rectifier for varying pulse widths (t) at the input. As the received pulse width is decreased, the slow response of the rectifier causes increased discrepancy between t_d and (t).

mode (when no wake-up signal is processed) [3, 41, 28]. The current consumption in sleep mode must remain as low as possible because the wake-up receiver typically remains idle for the majority of time. For example, we can see from [19] that the active current consumption is 25.68 mA and the sleep current consumption is only 10 μ A. Nevertheless, it can be shown that it contributes to almost half of the total average current consumption of the device, which is equal to 587 μ A for an average wake-up interval of 10 minutes. Therefore, the sleep mode current consumption must be reduced as much as possible.

The PWD circuit must remain active whenever input is received from the rectifier. When no signal is received from the rectifier, this could be due to lack of harvested energy, or the absence of a wake-up signal. Table 4.2 shows the current consumption of the components used in the PWD. To minimize the power consumption of the detector, a separate auto-power off timer is designed and tested to shutdown the detector when no signal is received from the rectifier. The auto-power off reduces the power consumption of the detector from a few microwatts to the nanowatt range. The active processing part of the PWD is powered through the power off circuit, and all the active components in Table 4.2 are powered OFF if no wake-up signal is received. The setup is shown in Figure 4.12. As an input pulse width is received, the passive front end of the PWD charges the capacitors.

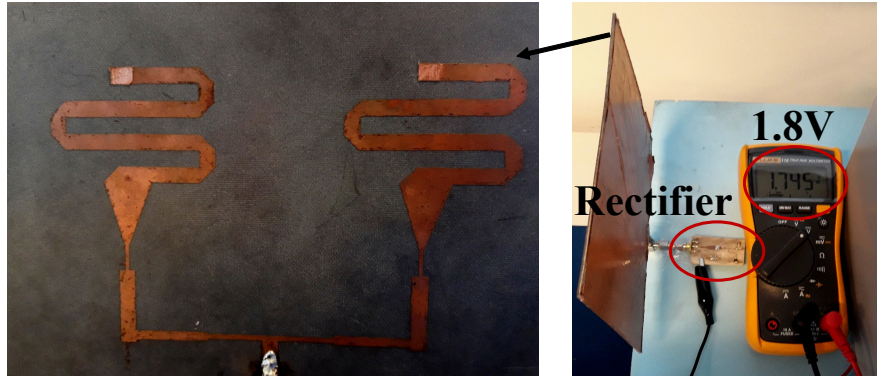


Figure 4.10: Experimental setup showing the transmitter placed 50 cm away from the wake-up receiver, with the width of the received pulse being processed by the designed pulse width detector

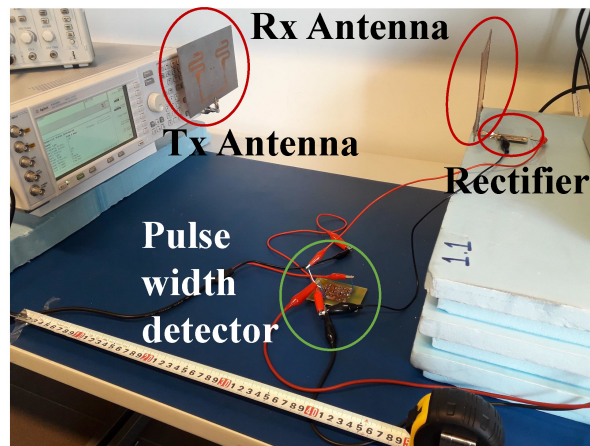


Figure 4.11: Rectenna system testing and output

Meanwhile, the same input is applied to the non-inverting comparator. The negative input V^- of the comparator is set to 50 mV through the voltage divider composed of R_1 and R_2 . Their values are equal to 1 M Ω , and 14.88 k Ω respectively with $V_{CC} = 3.3$ V. As capacitor C_3 charges, the output of the comparator goes HIGH and connects V_{CC} for the PWD through a power switch. The RC network at V^+ has a fast charging rate so that the output is turned on quickly when an input is received. On the contrary, the discharge rate is large. The PWD circuit

Table 4.2: Current Consumption of the PWD circuit @ 1.8 V

| Component | Quantity | Current Consumption |
|-----------|----------|---------------------|
| D-latch | 4 | 2 μA |
| Inverter | 1 | 0.5 μA |
| XoR Gate | 1 | 0.5 μA |

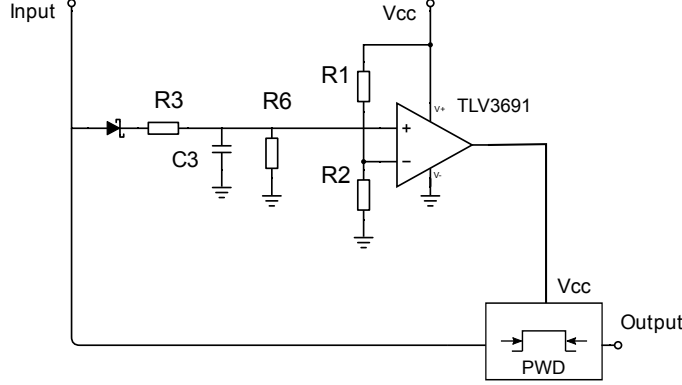


Figure 4.12: Auto power-off sleep circuit proof of concept

remains ON enough to generate an output after the pulsed wake-up is received. The values of the the RC network are set to $R_3 = 162 \Omega$, $C_3 = 4.7 \mu\text{F}$ and $R_6 = 1 \text{ M}\Omega$. The resulting shutdown timer is 14.6 seconds. This value can be tuned with the address value to ensure maximum energy savings. The comparator can source the current required by the PWD circuit or it can be used to control the operation of a voltage load switch.

4.1.2 Integration with an Agricultural Sensor

To increase the wake-up range beyond 50 cm, a data slicer circuit is integrated with the system to enhance sensitivity at the expense of increased power consumption. The system is then tested with an IoT sensor unit from Libelium to control the operation of a soil moisture sensor [5] [64].

The PWD circuit has the highest current consumption within the address detector. Therefore, its power supply is controlled by an auto-power off circuit, as shown in Figure 4.13. As a result, the only two components that remain permanently powered in the listening state are the data slicer and the auto-power off circuit. The PWD circuit is powered in the processing state to decide whether to

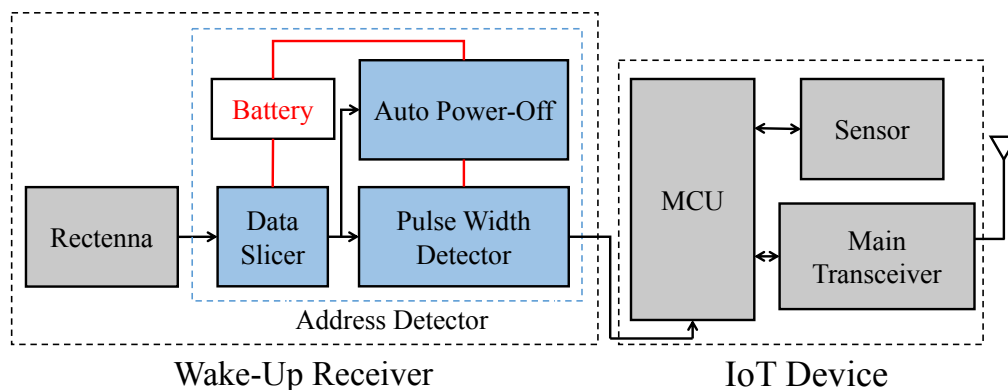


Figure 4.13: Block diagram showing the PWD integrated with an IoT sensor board (power lines shown in red)

trigger the sensor board. If the received wake-up signal matches the tuned width, the sensor board’s microcontroller is triggered, and it transitions from sleep mode to active mode. The sensor relays its measurements to the board, and the main transceiver is then switched ON to transmit data to a Wi-Fi access point. The board returns to sleep mode when data transmission is complete. In case of a mismatch, the address detector goes back to the listening state.

The address detector circuit is shown in Figure 4.14. It starts with a data slicer implemented using a TLV3691 comparator [65]. The negative input is configured with a threshold corresponding to a sensitivity of -30 dBm. The Sensitivity of the data slicer can be further increased, but this leads to increased susceptibility to noise as will be seen later. The data slicer is permanently powered ON by an LIR2032 3.6 V battery that provides the bias voltage for all active components. The voltage bias is delivered through a TPS78326 regulator [66] that maintains the bias to 2.6 V.

The address detector remains in the listening state as long as the width of the received input is below the low end of the tuned range. When the minimum level of the tuned range is reached, the voltage at the positive input of the auto-power off circuit and the logic threshold of the D pin of D-latch U1 exceeds the threshold (both are equal to 1.2 V). The auto-power off circuit switches ON the TPS22860 voltage-controlled switch [67], delivering V_{CC} to the PWD and the address detector moves into the processing state. The PWD is activated to check if the width of the input remains in the tuned range or exceeds it.

The auto-power off circuit disconnects power from the PWD after generating the trigger, switching the system back to the listening state. The threshold of the auto-power off unit is equal to that of the D-latch D1. Therefore, the PWD is not powered ON if the received signal falls below the tuned range. The auto-power off circuit does not switch power to the PWD in case of receiving fast, consecutive

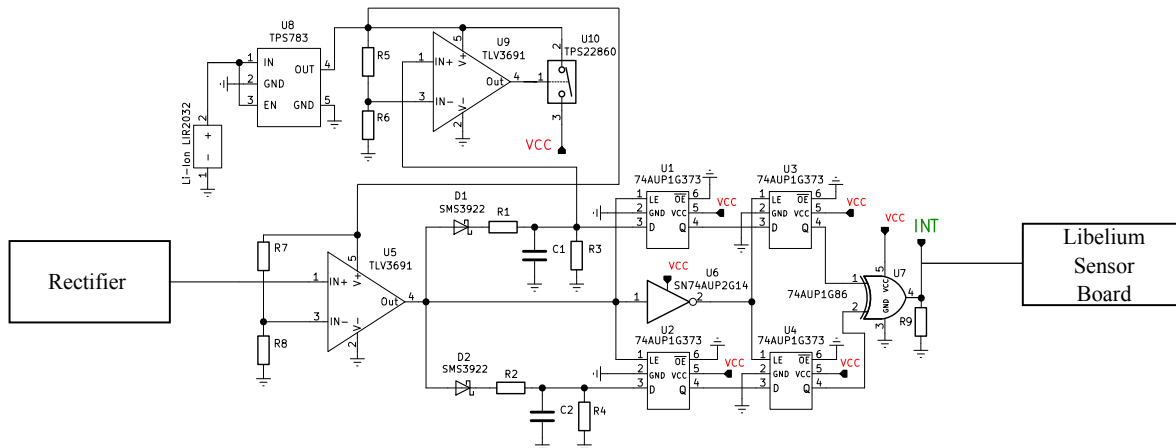


Figure 4.14: PWD integrated with and IoT sensor board circuit

pulses from the data slicer which enhances the circuit's noise immunity because this behavior is typical in a noisy environment, as will be seen in the experimental setup.

The system is integrated with a commercial smart agriculture wireless IoT unit from Libelium [5]. The IoT unit is composed of the main board (Waspote) which contains an ATmega1281 microcontroller [68]. The Waspote is connected to an agriculture sensor board as shown in Figure 4.16. It is powered by a single 3500 mAh li-ion battery, and contains a Wi-Fi module [69] and a 2.42 GHz antenna with a gain of 3 dBi. The mainboard is connected to a smart agriculture sensor board [4] that connects to a variety of agricultural sensors. The IoT unit is programmed to remain in sleep mode unless a trigger is received from the wake-up receiver on the ATmega1281 microcontroller's RXD1 port [68]. When a trigger is received, the main program is interrupted, and the main board switches to active mode where measurements are taken from a 200SS watermark sensor [70] (See Appendix B for interrupt code). The Wi-Fi module is then activated to connect to a nearby access point to transmit measurement data. The Wi-Fi module is turned OFF after transmission is complete, and the main board goes back to sleep mode leading to a significant decrease in power consumption.

Figure 4.15.a shows a sample output of a packet received from the soil moisture sensor. The packet includes different parameters, such as the frequency of the watermark sensor, the total number of wake-ups, timestamps, sensor battery level, and connection status. The watermark sensor reports a frequency value which varies with the water content in the soil. The frequency measurement can be converted to a soil water tension value (in cbar) or soil resistance (in Ohms) using the model shown in Figure 4.15.b [4].

Table 4.3 lists the active and sleep mode current consumption of the IoT unit

Sample Output

Initializing

Wake-up

Total # of wake-ups

1

Watermark1 Frequency: 8333.3330078125

Battery Level: 73 % | Battery (Volts): 3.9990000724 Volts

WiFi switched ON

WiFi set ESSID OK

WiFi set AUTHKEY OK

WiFi softReset OK

WiFi is connected OK

IP address: 192.168.1.124

GW address: 192.168.1.1

Network address: 255.255.255.0

Open UDP socket OK in handle: 0

Send Data OK

WiFi switched OFF

(a)

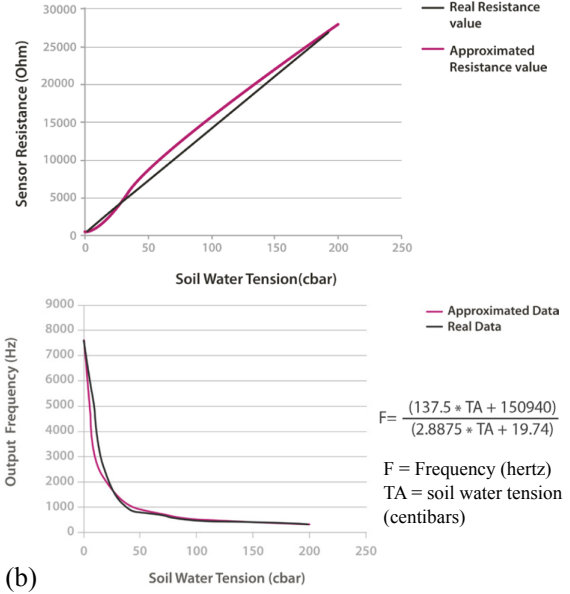


Figure 4.15: A sample output showing wake-up event and a soil moisture measurements. (b) Conversion between the frequency measurement and soil moisture [4]

(including the main board and the agriculture sensor board). It can be seen that the Wi-Fi module contributes the most to the total current consumption. Therefore, it is crucial to keep it in OFF state whenever data transmission is not taking place. The Wasp mote is therefore programmed to turn on the Wi-Fi module after obtaining sensor data and shutdown to reduce its current consumption.

4.1.3 Fabrication and Verification

The address detector circuit shown in Figure 4.14 is fabricated on an FR4 substrate. It has dimensions of 6.3 x 3.7 cm and a height of 1.2 mm as shown in Figure 4.17. It's characterized by a current consumption of 160 nA in the listening state and 3.16 μ A in the processing state. Table 4.4 lists the current consumption for all components in the listening and processing state. When compared with Table 4.3, the wake-up receiver's current consumption in the listening state is multiple orders less than the sleep mode current consumption of the Libelium IoT unit. Further, the detector remains in sleep mode unless while it is not processing a wake-up signal, leading to significant decrease in power consumption.

The values of the passive front-end are set to $R_1 = 197.3$ k Ω , $R_2 = 260.7$ k Ω , $R_3 = R_6 = 330$ k Ω , $C_1 = C_2 = 4.7$ μ F. This leads to generating a trigger whenever an input in the range of [800 - 1100] ms is received from the rectifier.

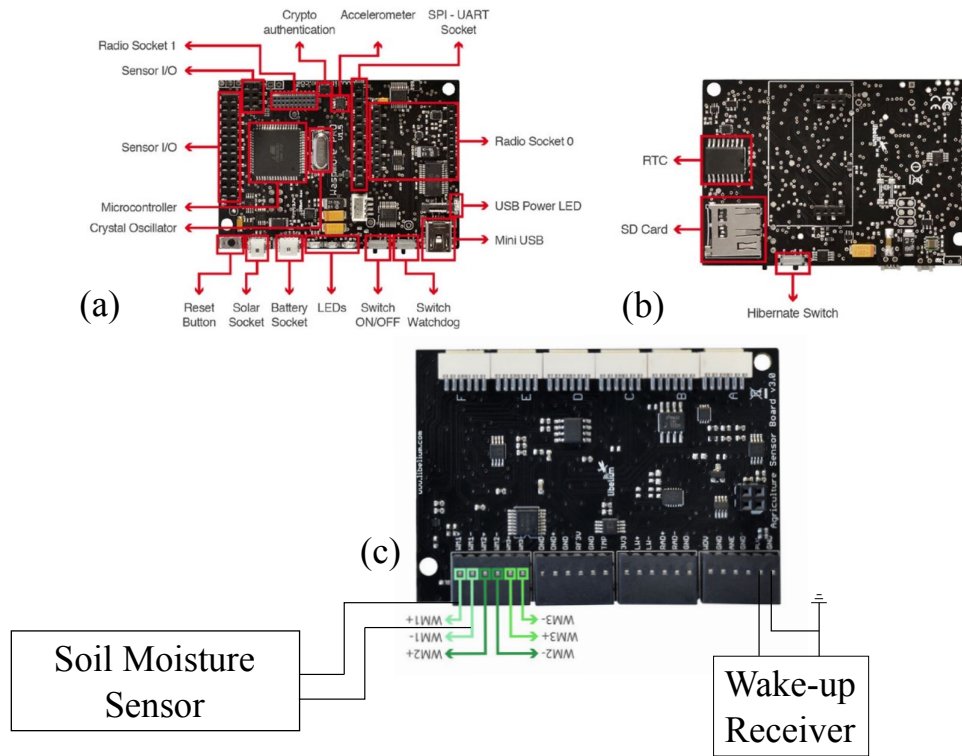


Figure 4.16: Integrating the Wake-up receiver with a Libelium IoT unit. (a) and (b) Main board showing labels for different components on the front and back sides, respectively [5]. (c) Agriculture sensor board providing interfaces to connect a variety of sensors [4]. The interrupt is generated through the PLV port that is connected to the ATmega1281 microcontroller's RXID port.

Table 4.3: Current Consumption of the Libelium IoT Unit

| Component | Sleep Current Consumption | Active Current Consumption |
|------------------------------|---------------------------|----------------------------|
| Wasp mote [5] | 33 μ A | 17 mA |
| Agriculture sensor board [4] | 0.8 mA | 0.8 mA |
| Wi-Fi PRO module [69] | 0 A | 350 mA |
| TOTAL | 0.833 mA | 367.8 mA |

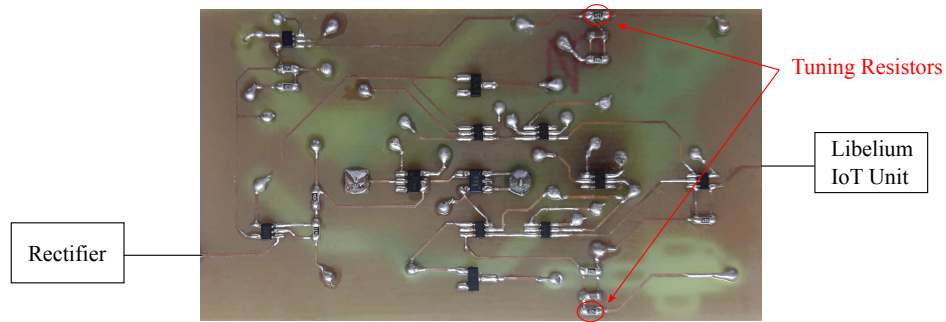


Figure 4.17: Fabricated address detector circuit.

Table 4.4: Current Consumption of the PWD-based Address Detector

| Component | Quantity | Current Consumption | Active in Listening State? |
|-----------------|----------|---------------------|----------------------------|
| Comparator [65] | 2 | 150 nA | YES |
| D-latch [59] | 4 | 2 μ A | NO |
| Inverter [71] | 1 | 0.5 μ A | NO |
| XoR Gate [61] | 1 | 0.5 μ A | NO |
| Switch [67] | 1 | 10 nA | YES |
| Regulator [66] | 1 | 500 nA | YES |

4.1.4 Experimental Setup and Router-Initiated Wake-up

The use of a Wi-Fi access point as the wake-up transmitter offers many advantages over dedicated due to the prevalence of Wi-Fi access points. In this section, we show that a commercial Wi-Fi router can be used to transmit a wake-up signal without medication to its software or hardware. The wake-up signal can be demodulated and processed using the PWD previously proposed. A block diagram of the experimental setup of access point-initiated wake-up is shown in Figure 4.18. The period of the burst (number of packets) determines the transmitted address. This burst is modulated as an OOK RF signal and transmitted through the antenna. The wake-up receiver demodulates this signal into pulses and processes the width.

The IoT unit is connected to a soil moisture sensor [70] that measures the water content of the soil once activated by the wake-up receiver. The Libelium IoT unit authenticates with the access point and transmits the measurement value. Therefore, the same access point is used to transmit the wake-up signal and receive the data from the sensor. The address is controlled by varying the number of

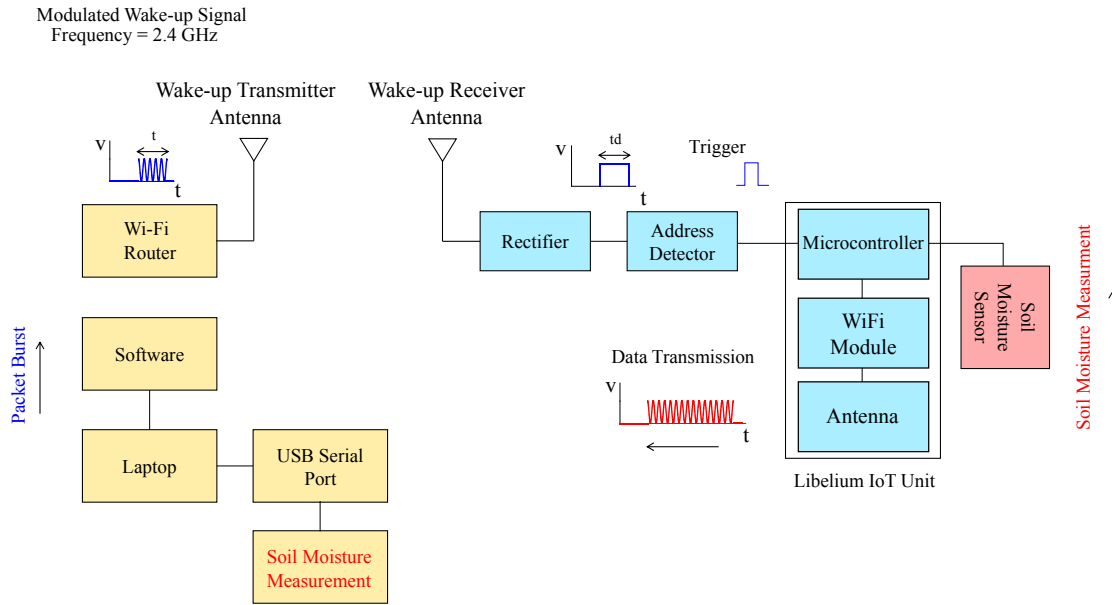


Figure 4.18: Block diagram of the experimental setup using a commercial router as the wake-up transmitter

packets, and the wake-up receiver is tuned by varying the value of the tuning resistors shown in Figure 4.17.

Figure 4.19(a) shows the experimental setup for wake-up from a commercial router [72]. The wake-up transmitter and wake-up receiver are separated by a distance of 3 meters to test selective wake-up operation. The transmit power at the wake-up transmitter is set to 7 dBm. To convey a wake-up signal, a burst of 802.11n frames, each having a standard size of 1,044 bytes, is generated using a packet builder software [73]. This burst is modulated into an RF signal for a specific period which is transmitted by the antenna.

The wake-up receiver (Figure 4.19.(b)) detects the burst of packets and generates a trigger. In this setup, we tune the PWD to generate a trigger when a burst of [100 - 140] packets is received and generates a pulse with a width of [800 - 1100] ms at the rectifier's output. An inter-frame spacing (IFS) of 0.1 ms is inserted between the frames. This value is chosen large enough to avoid congestion at the transmitter's output, while small enough to maintain a stable, uninterrupted pulsed signal at the input of the wake-up receiver.

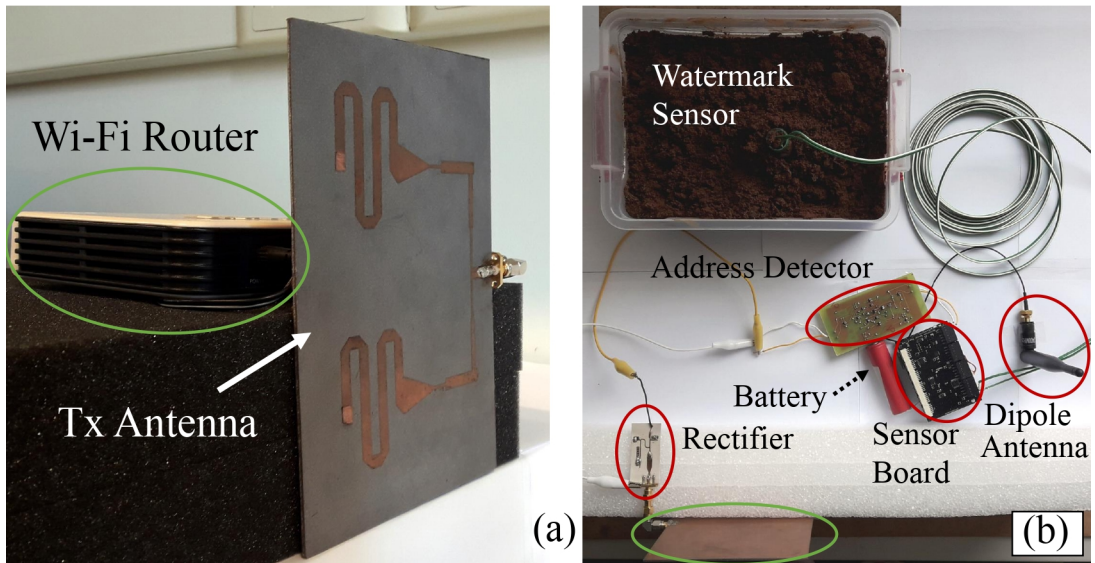


Figure 4.19: Experimental setup for testing wake-up from a commercial Router. (a) Wake-up transmitter composed of a Wi-Fi Router and An antenna. (b) Wake-up receiver composed of an antenna, rectifier, and address detector. The Wake-up receiver activates the IoT Libelium sensor unit that transmits data using a dedicated antenna

4.1.5 Evaluation and Discussion

In a noise-free environment, the wake-up signal is transmitted 100 times with a successful wake-up rate of 96%. However, in a real-world application, the Wi-Fi router communicates with several other wake-up receivers and users connected for regular Wi-Fi activity. Therefore, signals transmitted by the router are seen as noise by the wake-up receiver and lead to generating false wake-ups.

To test the effect of operating the system in a noisy environment, wake-up signals are transmitted, and the wake-up event is monitored in different conditions. To generate a noisy environment, a Wi-Fi user connects to the Wi-Fi router and exchanges regular data with the laptop through the Wi-Fi connection. The interfering user's transmit power is varied between 7 and 13 dBm to mimic mobility.

The output of the data slicer with the interfering user in the vicinity of the WuRx is shown in Figure 4.20. The noisy environment generates a train of variable-width pulses at the input of the pulse width detector, which processes each pulse as a wake-up signal with a unique address. False wake-ups occur when a pulse in the tuned range of [800 – 1100] ms is received. Under the noisy conditions, 100 wake-up signals are generated at random times. However, due to noise at the output of the data slicer, the successful wake-up rate falls to 59%. Furthermore,



Figure 4.20: data slicer's output in a noisy environment

connecting the interfering user to the network results in 252 false wake-ups during 10 hours of connectivity, and a false wake-up probability of 6.23%.

The lifetime of the sensor board is a crucial parameter that determines its applicability in real-world applications. In order to assess the lifetime, the total current consumed by the sensor board can be calculated by taking into consideration all the possible states of the system and their respective current consumption. For this system, the current consumption is found as follows:

$$I_T = D_{ON}I_{ON} + (1 - D_{ON})I_{ON}P_F + (1 - D_{ON})(1 - P_F)I_S \quad (4.2)$$

where D_{ON} is the fraction of time that the IoT unit spends in active state, I_{ON} and I_S are the active and sleep mode currents in Table 4.3 and P_F is the false wake-up probability. The value of D_{ON} for a given trigger rate, $T_{trigger}$ can be calculated as:

$$D_{ON} = T_{ON}/T_{trigger} \quad (4.3)$$

Where T_{ON} is the average time that the sensor board spends in active mode after being triggered. In the experimental setup provided in the previous section, this time is found to be 8.9 seconds in a noise-free environment. The lifetime of the sensor board is found as:

$$T = C(mAh)/I_{total}(mA) \cdot 0.7 \quad (4.4)$$

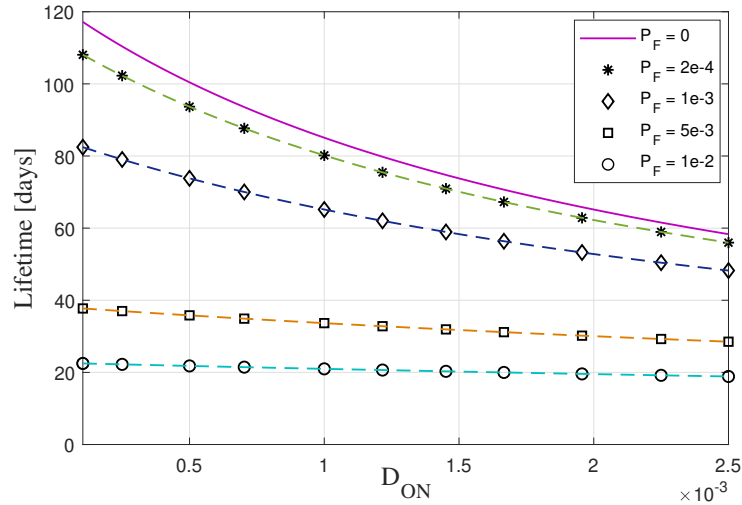


Figure 4.21: Lifetime of the IoT sensor unit for different values of false wake-up probability

Where C is the battery capacity, and a factor of 0.7 is used to model external factors affecting the lifetime of the battery.

Figure 4.21 shows the predicted lifetime of the IoT unit as a function of D_{ON} where the average trigger rate is varied between 30 minutes and 24 hours. Multiple plots are provided for different values of P_F . The false wake-up probability significantly influences the average current consumption of the IoT sensor unit and should be reduced as much as possible. Nevertheless, this reduction cannot be achieved without an increase in the complexity and current consumption of the wake-up receiver.

In an ideal scenario, wake-up receivers are integrated to increase the lifetime of sensors compared to scheduled wake-ups. The increase in the lifetime depends on the application and the false wake-up probability when implementing a wake-up receiver. Implementing a wake-up receiver leads to increased lifetime only if the false wake-up probability is low. Meanwhile, scheduled wake-ups do not suffer from this issue because the wake-up trigger is generated internally.

We can highlight the benefit of implementing a wake-up receiver when compared to scheduled triggers by considering the greenhouse application provided in [14]. It is shown that the water consumption of a plant over 50 days can be divided into three periods. Based on the data provided in [14] and presented in Table 4.5, the water consumption increases during a plant's lifespan, which typically requires a varying rate of measurements over time. In the case of scheduled wake-up, the trigger rate must be set to the highest value needed throughout the plant's lifes-

Table 4.5: Measurement frequency for scheduling and WuRx

| Period (days) [14] | Average Water Consumption [14] | D_{ON} WuRx | D_{ON} Scheduled |
|--------------------|--------------------------------|---------------|--------------------|
| 0 - 10 | 400ml/day | 0.03% | 0.25% |
| 11 - 30 | 600ml/day | 0.0625% | 0.25% |
| 31 - 50 | 750ml/day | 0.25% | 0.25% |

Table 4.6: Comparison of sensor board lifetime

| Condition | Scheduled | WuRx $P_F = 0$ | WuRx $P_F = 2e-4$ | WuRx $P_F = 1e-3$ | WuRx $P_F = 2e-3$ |
|-----------------|-----------|-------------------|----------------------|----------------------|----------------------|
| Lifetime (days) | 58.32 | 77.65 | 73.72 | 60.67 | 50.04 |

pan if reprogramming the unit is not feasible. However, this leads to unnecessary wake-ups in the other two periods, which require less frequent measurements.

On the other hand, implementing a wake-up receiver allows controlling the trigger rate over the 50 days resulting in a smaller average D_{ON} (0.13%). The result is a longer lifetime when compared to scheduling, as shown in Table 4.6. Nevertheless, implementing a wake-up receiver suffers from the disadvantage of a high false wake-up rate, which can lead to a higher average current consumption when compared to scheduled wake-up. This increase in the average current consumption contradicts with the main motivation of integrating a wake-up receiver. Therefore, the main two objectives of the rest of this work are: 1) increase the address space beyond a pulse width detection. This scheme achieves addressing by varying values of passive components but suffers from an exponential increase in the pulse width as the number of addresses is increased. 2) Reduce the false wake-up probability while maintaining simplicity in the design of the address detector and a listening current in the nano-range.

4.2 Multi-Power-Mode Address Detector Design

Extending the address range of the address detector requires additional hardware that increases its overall current consumption. In this section, we consider the concept of a power state machine to expand the address range and maintain a listening current in the nano-amp range [74] [75]. The address detector switches

between multiple power modes to process the demodulated signal while it scans for the configured wake-up signal. By considering the available modulation schemes in Table 4.1, the address range can be extended by adding PWM-modulated 0- and 1-bits that follow the initial pulse with a specific width. The bit correlator hardware required to demodulate the PWM-modulated bits is added to the circuit developed in the previous section. The pulse composed of a specific width serves as a coded preamble to indicate that a bit stream will follow and avoid powering ON the bit correlator whenever the input exceeds the data slicer's threshold.

4.2.1 System Block Diagram and Multi-State Operation

Figure 4.22 shows a block diagram of the multi power state system implementing combined harvesting and wake-up operations. The wake-up transmitter transmits signals to charge the battery and wake-up the device located at the receiver side. It switches between charging and wake-up operations by transmitting continuous and modulated signals as shown in Figure 4.23. On the other hand, the address detector and harvester receive both continuous and modulated signals when sharing an antenna and rectifier. Receiving the modulated signal does not impact the harvester's performance. In fact, the harvester continues to charge the battery while the modulated signal is received. On the other hand, receiving the continuous signal is detrimental to the address detector because it switches to higher power modes and treats the input as a wake-up signal. For example, the PWD discussed in the previous section treats the received continuous signal as an input pulse and remains powered ON to process its width. This leads to wasted energy especially if charging tasks are conducted for long periods. To overcome this issue, we introduce an RX/harvesting switch to shutdown address processing while the device is charging.

The wake-up signal of the multi power state detector is composed of the following elements:

- A coded preamble generated by a signal burst at f_0 GHz that lasts for a specific period, as discussed in Section 4.1. The preamble's width determines its unique code
- The preamble is followed by a guard time with a period of $g1$ [seconds]
- An 8-bit sequence composed of Pulse Width Modulation (PWM) modulated bursts at f_0 GHz with two distinct periods representing a 0- or 1-bit
- The bit bursts are separated by a guard time with a period of $g2$ [seconds]

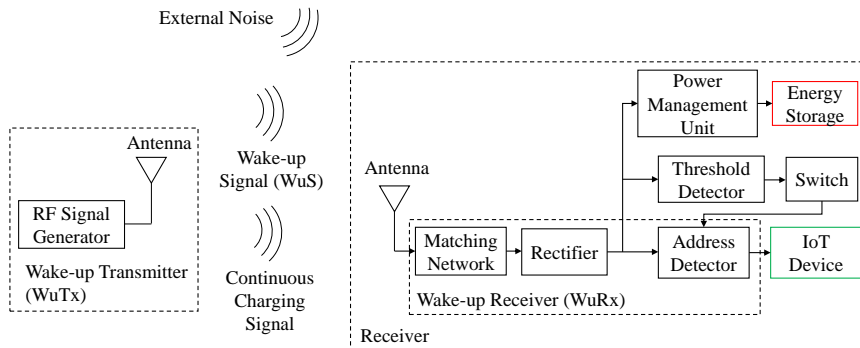


Figure 4.22: System block diagram showing a wake-up receiver with combined RX and harvesting configuration

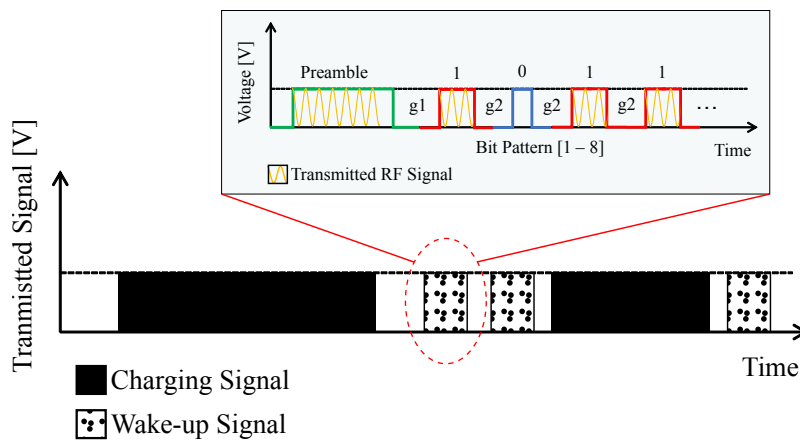


Figure 4.23: Charging and wake-up signals transmitted by the WuTx. The WuTx can switch between the two operating modes by transmitting continuous and modulated signals.

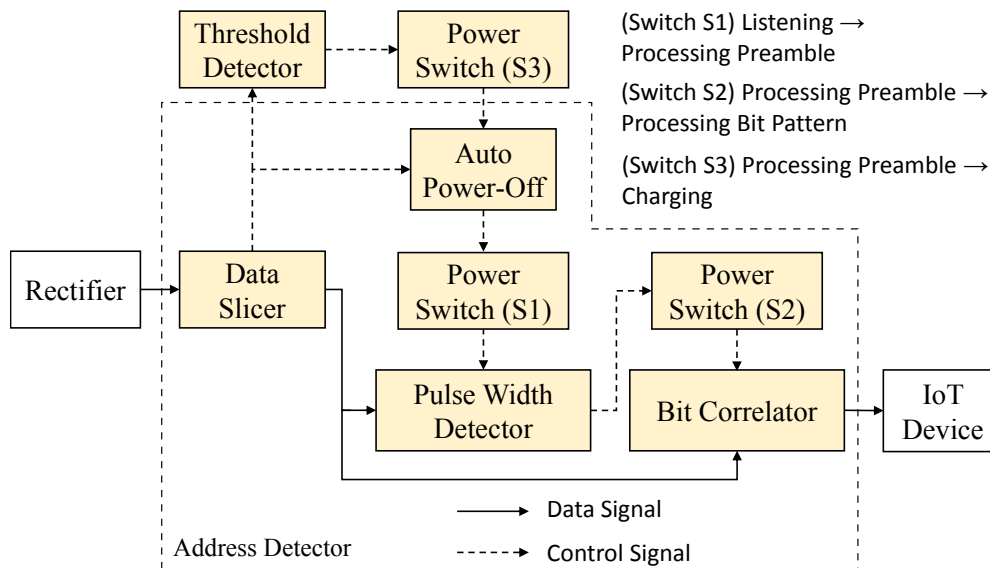


Figure 4.24: Address detector block diagram

A block diagram of the multi-power-state address detector is shown in Figure 4.24. The detector is composed of several units responsible for detecting the WuS and controlling power delivery to active components. It includes the PWD circuit described in Section 4.1 and a bit correlator that is activated only if the PWD matches the preamble. Additionally, a threshold detector is used as an RX/harvesting switch to power OFF the address detector during charging.

In addition to the listening and processing preamble states introduced in Section 4.1 the full address detector operates with two additional states as shown in Figure 4.25. The power consumption of the detector gradually increases as the WuS is processed. It remains in the *listening* state when no signal is received from the rectifier and reduces its current consumption to the nano-amp range. When a signal with an amplitude exceeding the threshold of the data slicer is received, the auto-power off timer connects power to the PWD to process the width of the pulse, and the detector moves to the *processing preamble* state. This state is maintained until the preamble is fully received, i.e. at the start of $g1$. The PWD connects power to the bit correlator if the received pulse width is matched, and the detector moves to the *processing bit sequence* state. Conversely, the circuit returns to the listening state if the received pulse is not matched. In the processing bit sequence state, the bit correlator inspects the bit sequence to determine if it matches the tuned sequence. It generates a trigger to the IoT device when the bit sequence is matched. The threshold detector shuts down the circuit during charging operations, reducing its current consumption to the nano-amp range. When

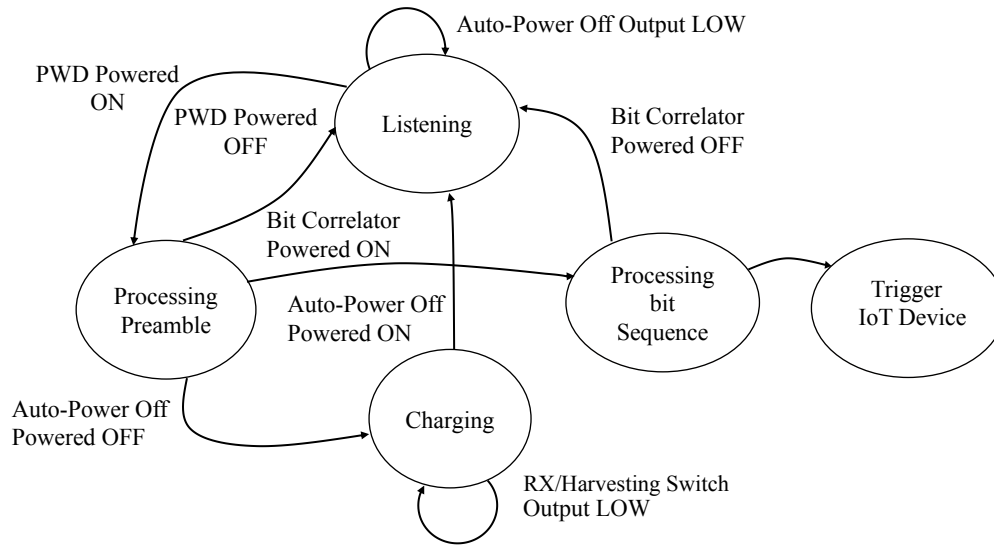


Figure 4.25: Address detector power consumption states. The circuit constantly spins in a power state machine to reduce the average current consumption

the input signal causes the RX/harvesting switch to exceed its threshold, power is disconnected from the auto-power off timer, effectively shutting down the address detector while the system is charging its energy storage. The RX/harvesting switch is designed to avoid powering OFF the address detector when a WuS is received by controlling the value of guard time g_2 . Power is connected to the auto power off timer and the address detector returns to the listening state when the charging task is completed.

Table 4.7 summarizes the units activated in each power state. The peak current consumption is reached during the processing bit sequence state where all components are activated. On the other hand, current consumption is minimized during the listening and charging states as the detector shuts down the majority of active components.

4.2.2 Multi-Mode Address Detector Circuit

In this section, the operation of the full address detector circuit is described in each power state. The detector circuit is shown in Figure 4.28. The circuit diagram is divided into logical units showing the different components of the detect. In addition, specific points are highlighted in the diagram as testing probes for experimental verification.

Table 4.7: Address Detector Power States

| State | Active Components |
|-------------------------|--|
| Listening | Data slicer; Auto-power off; RX/harvesting switch |
| Processing Preamble | + PWD |
| Processing Bit Sequence | + Bit correlator |
| Charging | RX/harvesting switch; Data slicer |

Operation in the listening state

As mentioned in Section 4.1, only minimal components are powered on when listening to the medium to detect a signal with a strength that exceed the detector's threshold. The input of the circuit is connected to the output of a rectifier. The data slicer is implemented in nanopower comparator $C1$ [65] with the positive input connected to the rectifier and it is permanently powered on. The negative input is configured with a threshold using the voltage divider of R_9 and R_{10} .

Operation in the processing preamble state

Operation in this state is similar as described in Section 4.1. The pulse width detector (operating as a preamble detector) generates a high edge when a preamble with the tuned width is received. The output of the PWD, however, controls power delivery to the bit correlator through $S3$, to move the circuit to the processing bit sequence when the pulse width is matched.

Another modification to the PWD circuit is required to avoid shutting down the bit correlator when the first bit is received. An RC circuit is connected to the (EN) pins of $D1$ and $D2$. The D-latches are only enabled if the voltage at R_8C_3 exceeds the threshold (see Figure 4.26, t_2). The bit sequence is composed of pulses with a period shorter than the shaded area (between t_1 and t_2). The D-latches are therefore not enabled when the bit sequence is received.

Operation in the processing bit sequence state

In the processing bit sequence state, the bit correlator demodulates the PWM-modulated 1- and 0-bits and their values are stored in parallel in a shift register [76]. A demodulator composed of an RC circuit and one active component, inverter

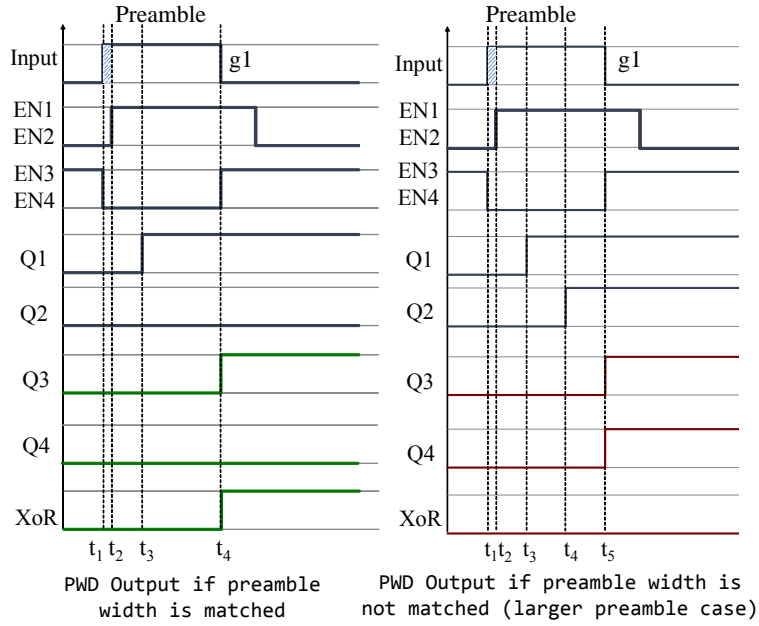


Figure 4.26: Modified PWD operation to avoid shutting down the bit correlator when receiving the bit sequence

N_2 , is connected to the shift register. The clock of the shift register is controlled by inverting the input bit sequence, as shown in Figure 4.27. The value recorded on $R_{15}C_5$ is pushed to the serial port after the bit is removed, i.e. at the start of g_2 , and the value of g_2 is selected such that the $R_{15}C_5$ fully discharges before the following bit is received. The $R_{15}C_5$ voltage remains below the threshold of the shift register's serial port when a 0-bit is received, but it exceeds the threshold when a 1-bit is received. Logic gates are connected to the shift register's parallel output to generate a trigger when the bit sequence is matched. After generating a trigger, the R_7C_1 circuit discharges and power is disconnected from the PWD and the bit correlator. The detector returns to the listening state.

Experimental results of the bit correlator operation are shown in Figure 4.31. The figure shows the received bit sequence, the demodulated signal, extracted clock, and a trigger generated when the correct bit sequence is received.

Operation in the charging state

The address detector is configured to shut down the PWD and the bit correlator during charging operations. Upon charging, the voltage on R_2C_2 exceeds the threshold of the RX/harvesting switch configured on the negative input of com-

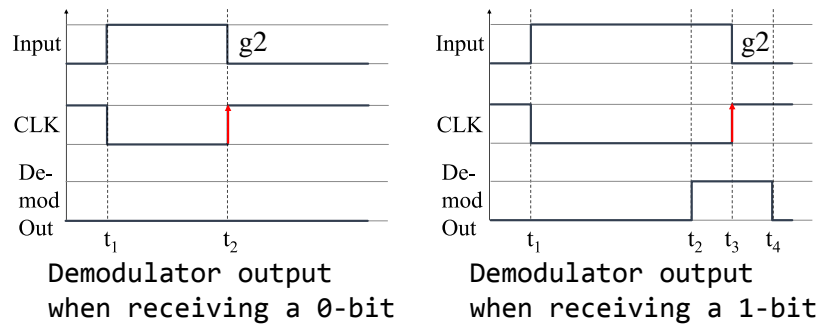
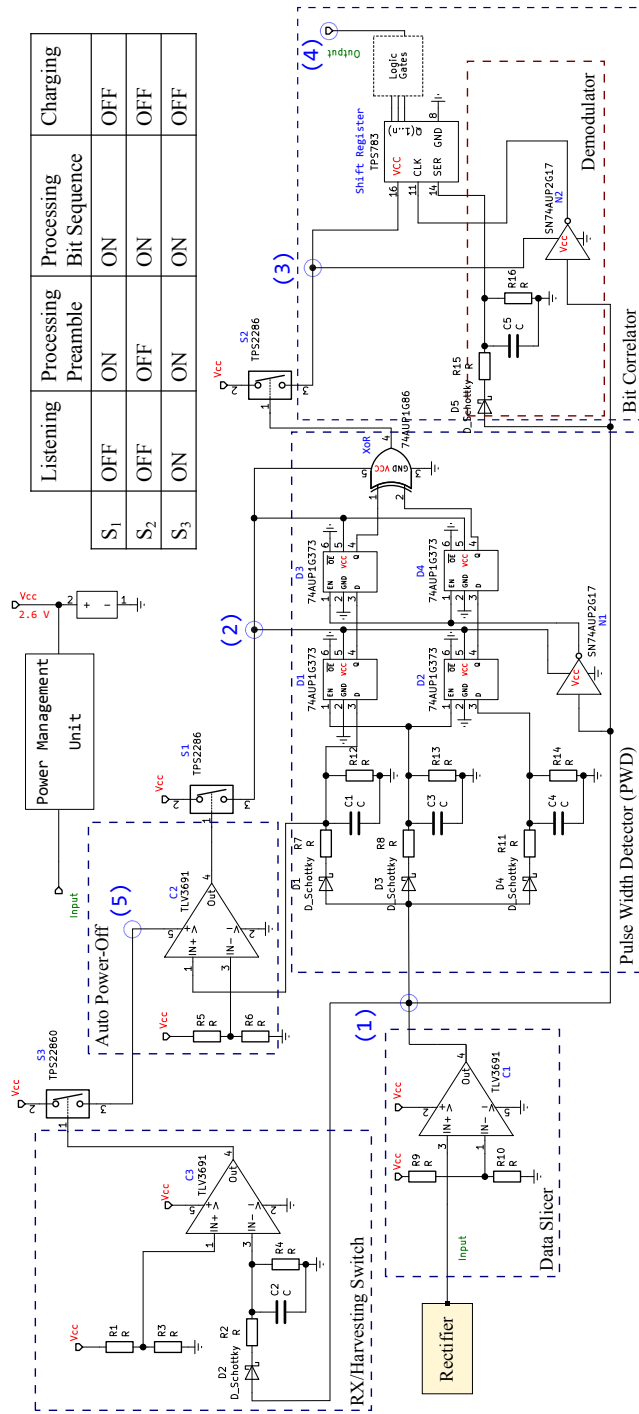


Figure 4.27: Demodulator operation. Demodulating the 0- and 1-bit is achieved by inverting the input sequence. The voltage determines the decoded value

parator $C3$. The switch is a threshold detector configured with negative logic. It disconnects power from the auto-power off circuit when the threshold is exceeded. The R_2C_2 circuit discharges after the WuTx completes the charging operation, allowing the address detector to return to the listening state.



| | Listening | Processing Preamble | Processing Bit Sequence | Charging |
|----------------|-----------|---------------------|-------------------------|----------|
| S ₁ | OFF | ON | ON | OFF |
| S ₂ | OFF | OFF | ON | OFF |
| S ₃ | ON | ON | ON | OFF |

Figure 4.28: Multi-power-mode Address detector circuit schematic

4.2.3 Multi-power Mode Address Detector Fabrication and Testing

Current consumption, sensitivity, and data rate

The address detector is fabricated on an FR4 substrate, and it is shown in Figure 4.30. The prototype operates at a bias voltage of 2.6 V. Our previous work demonstrated that the address detector circuit is characterized by a sensitivity of -40 dBm when combined with the rectifier designed and implemented in [55]. The combination achieves a wake-up distance of 27.5 meters at a transmit power of 15.4 dBm [77].

The designed multi power state system leads to a significant reduction in the circuit's current consumption. Figure 4.29 demonstrates the distribution of the maximum current consumption of $I_{max} = 13.725 \mu\text{A}$ realized during the processing bit sequence state where all units are activated. The bit correlator contributes to 76.3% of I_{max} . Therefore, shutting down the bit correlator offers major power savings. The current consumption is reduced to 225 nA during the listening state. This value amounts to a decrease of 98% from the processing bit sequence state. Furthermore, implementing a coded preamble enhances noise immunity by avoiding the activation of the bit correlator component whenever the input signal level exceeds the circuit's minimum threshold. The circuit switches to the processing preamble state with a moderate current consumption, amounting to less than 25% of I_{max} to detect the input pulse width instead of immediately activating the bit correlator. The circuit only reaches its I_{max} after the preamble is matched, indicating the reception of a wake-up signal.

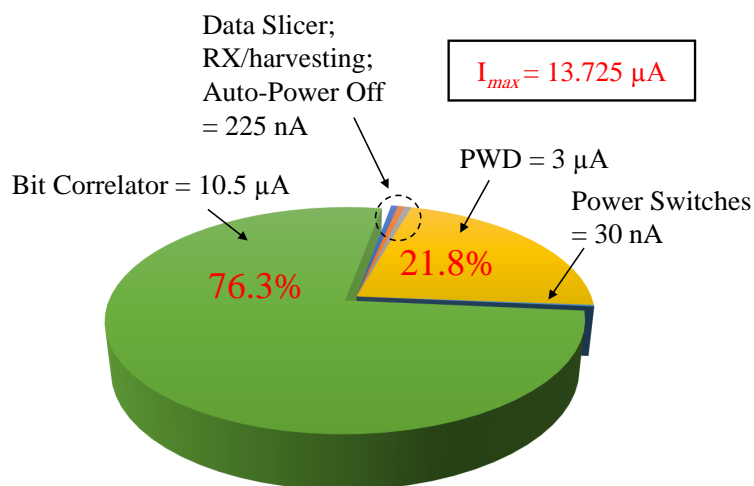


Figure 4.29: Allocation of the total current consumption between various components.

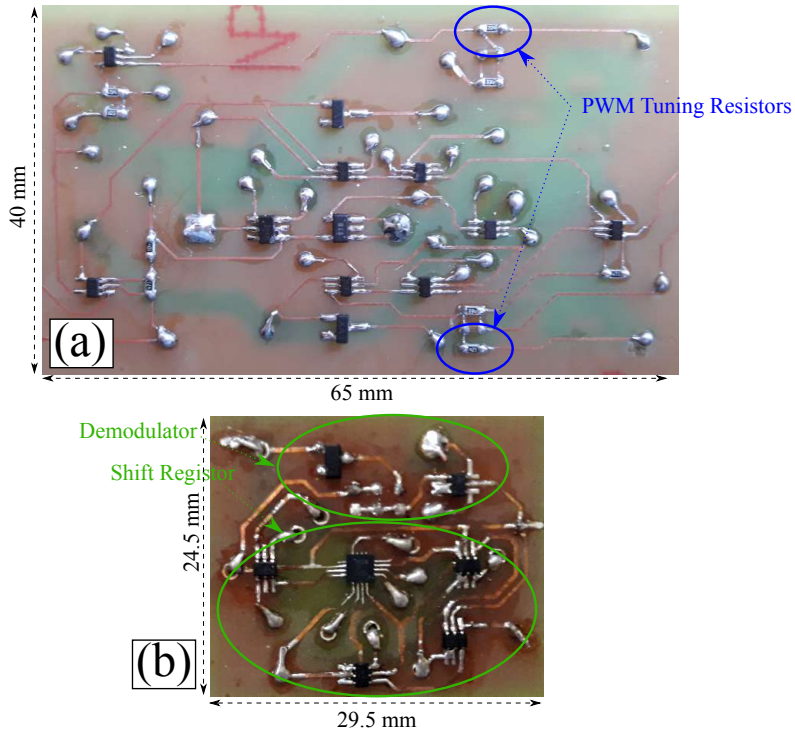


Figure 4.30: Fabricated prototype including a) pulse width detector. b) bit correlator

The data slicer introduces a limit on the address detector's maximum data rate due to the slow response time of the comparator [65] to the input signal's rise and fall. The slow response negatively affects the integrity of the demodulated preamble pulse width and bit sequence. Specifically, the slow response time causes a widening of the data slicer's output for input pulses with fast rise and fall time, as shown in Figure 4.32. The minimum detectable input pulse duration is experimentally found to be 200 μsec so the 0- and 1- bits can be modulated as a 250 μsec and 500 μsec pulses, respectively. In addition, a minimum guard time of $g2 = 3T_{bit} = 1.5 \text{ msec}$ is required to fully discharge the $R_{15}C_5$ circuit, where T_{bit} represents the duration of the 1-bit. Therefore, the system can achieve a maximum data rate of $\frac{1}{(0.5+1.5) \text{ ms}} = 500 \text{ kbps}$.

Multi-power operation experimental results

Multi power state operation is demonstrated by tuning the address detector to the WuS with the specifications provided in Table 4.8. The address detector is configured with the values shown in Table 4.9 to generate a trigger when that WuS is received.

Figure 4.33.a exhibits the detection of the WuS and the generation of a trigger

when the preamble and the bit pattern are matched. The bit sequence is terminated with a 0-bit because the bit correlator unit [76] contains a storage register that lags one clock cycle behind the shift register. Signal (1) in Figure 4.33.a shows the detector operating in the listening state before receiving a WuS with the specifications in Table 4.8. The auto-power off circuit connects power to the PWD as seen in Signal (2) and the detector moves to the processing preamble state. Signal (3) shows connecting power to the bit correlator after the preamble is fully received, at the start of g_1 . In the processing bit sequence state, the bit pattern is correlated and a trigger is generated when this bit sequence is matched, as seen in Signal (4). The detector returns to the listening state after generating a trigger. The R_7C_1 circuit discharges and power is disconnected from the PWD and the bit correlator. Signal (5) shows the output of the RX/harvesting switch. It can be seen that the output remains high, indicating that the auto-power off circuit is powered.

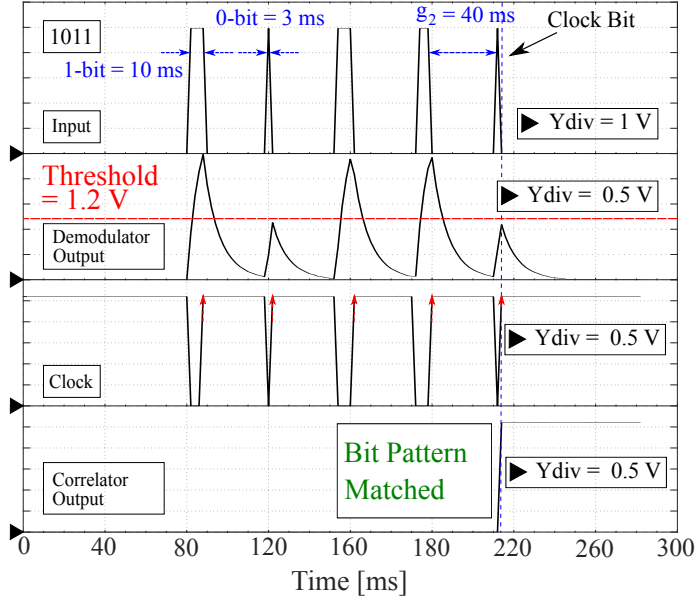


Figure 4.31: PWM bit demodulation at 20 *kbps*. The bit value is determined by the voltage value recorded on $R_{15}C_5$

The address detector processing preamble state then goes back to listening state if the preamble is not matched. This is shown in Figure 4.33.c and Figure 4.33.d. The address detector switches to the processing preamble state as the previous case in Figure 4.33.a. However, since the preamble width is not matched, no control signal is generated by the PWD to power the bit correlator, and the address detector moves back to the listening state. On the other hand, Figure 4.33.b exhibits receiving a WuS that begins with the correct preamble followed by an

erroneous bit sequence (1111). The address detector switches from listening to processing preamble to processing bit sequence, but no trigger is generated because the bit sequence is not matched.

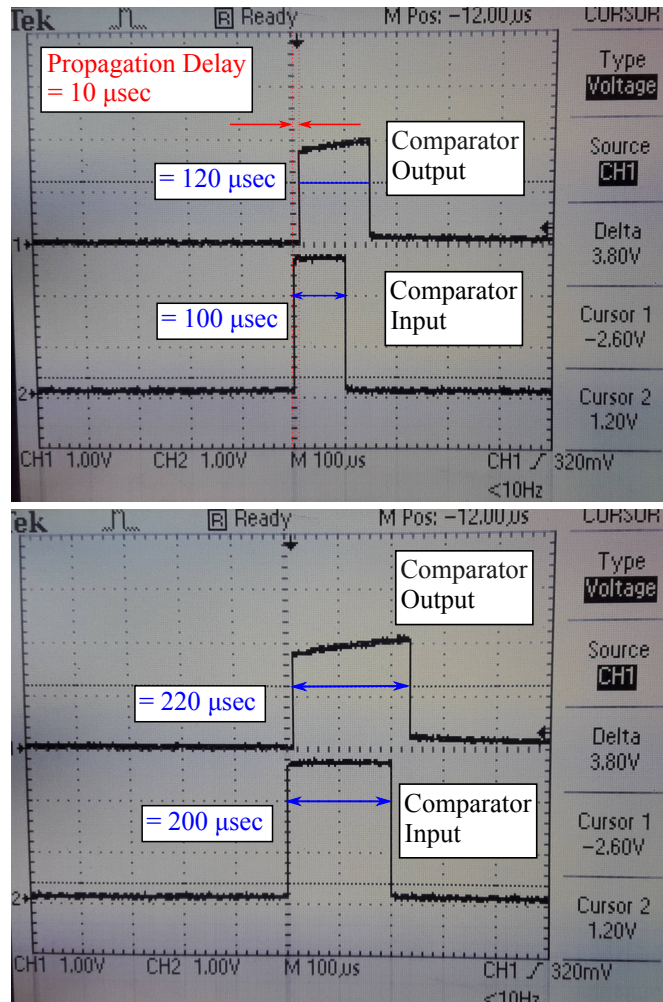


Figure 4.32: Comparator propagation and response time. (top) Response time for an input pulse of $100\mu\text{sec}$ causing distortion at the output (bottom) As the input pulse increases, the comparator's time causes less significant distortion

When the WuTx is conducting a charging task, the address detector receives a continuous signal from the rectifier as shown in Figure 4.33.e. The figure shows receiving a continuous charging signal for a period of 6 seconds. The charging signal is first treated by the address detector as a WuS. When the voltage exceeds the threshold of the RX/harvesting switch, its output turns low and disconnects power from the auto-power off timer. The detector moves to the charging state and remains in that state as long as the R_2C_2 voltage remains above the threshold.

Table 4.8: Wake-up Signal Tuning of the Fabricated Prototype

| Component | Value |
|-----------------|--------|
| Preamble | 300 ms |
| Guard time $g1$ | 300 ms |
| Guard time $g2$ | 40 ms |
| 1-bit | 10 ms |
| 0-bit | 3 ms |

Table 4.9: Component Values of Fabricated Prototype

| Component | Value |
|-----------------------------|-----------------|
| Data slicer | |
| R_9 | 1 k Ω |
| R_{10} | 120 k Ω |
| Auto-power off | |
| R_5 | 10 k Ω |
| R_6 | 8.2 k Ω |
| PWD | |
| R_7 | 13.8 k Ω |
| R_{11} | 2.24 k Ω |
| R_8 | 45 k Ω |
| $C_1; C_3; C_4$ | 15 μF |
| $R_{12}; R_{13}; R_{14}$ | 100 k Ω |
| RX/harvesting switch | |
| R_2 | 45 k Ω |
| C_2 | 15 μF |
| R_4 | 100 k Ω |
| R_1 | 15 k Ω |
| R_3 | 10 k Ω |
| Demodulator | |
| R_{15} | 1 k Ω |
| C_5 | 1.5 μF |
| R_{16} | 15 k Ω |

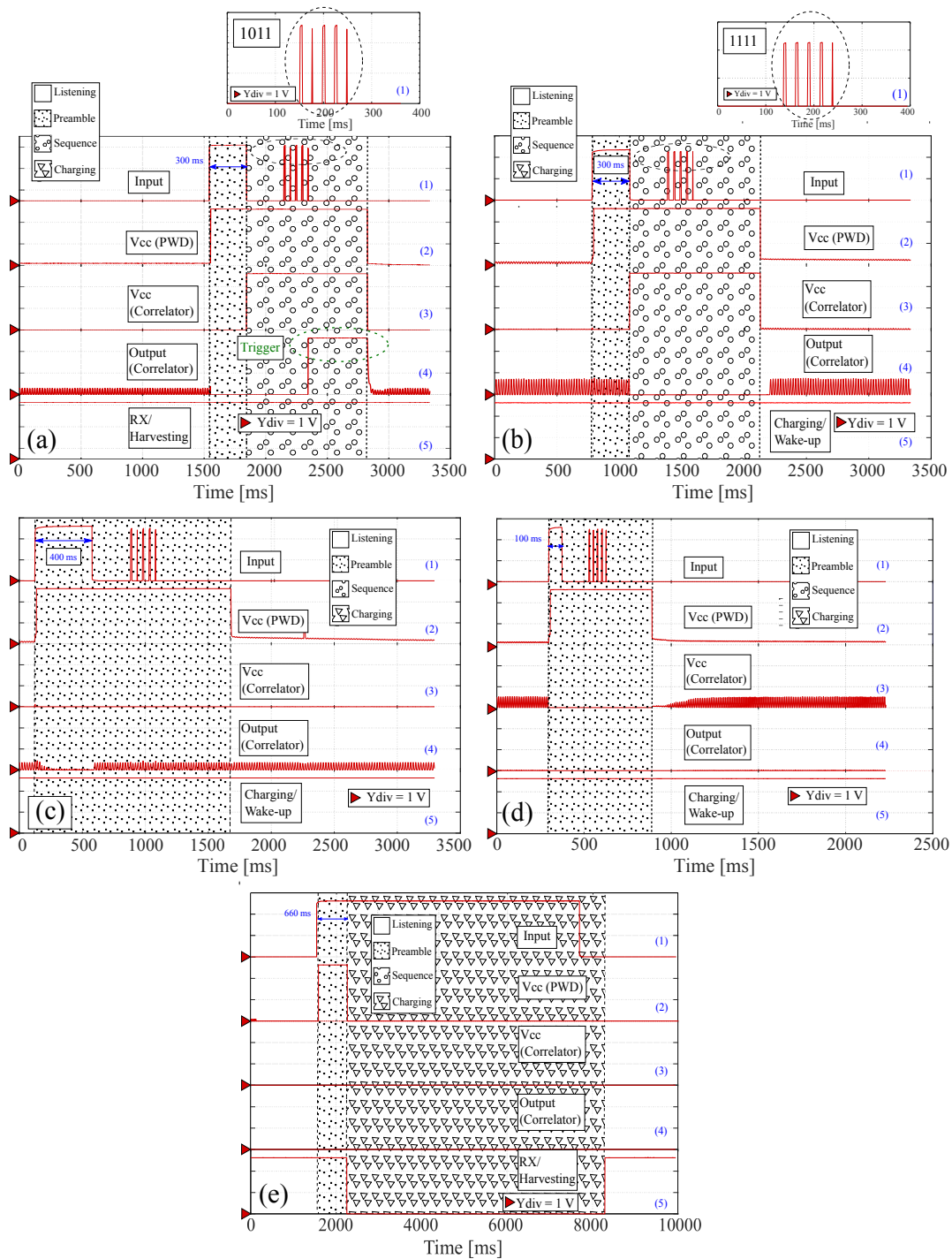


Figure 4.33: Address detector multi-power-state operation

Chapter 5

Analytical Results

In this chapter, we provide an analytical discussion to estimate the average current consumption of the proposed address detector. Unlike other solutions available in the literature, the proposed design has multiple power states and its average current consumption depends on a number of factors including external noise, average charging time, and wake-up signal tuning. All these variables influence the average current consumption which can take any value up to the maximum of $13.772 \mu\text{A}$ obtained when all components are operating. We demonstrate that the multi-power architecture reduces the current consumption when compared to the two-state approach. In addition, we show that the proposed architecture is characterized by a higher noise immunity which reflects in smaller current consumption when operating in noisy environments.

5.0.1 Average Current Consumption of the Address Detector in a Noise-Free Environment

Active current consumption

In this section, we consider the current consumption required to process one wake-up signal and the detector's average current consumption for different wake-up signal configurations including bit rate, address size, and preamble width. For two-state address detectors, the active current consumption has a significant contribution to the average current consumption where the address detector reaches its maximum current consumption. On the contrary, our proposed address detector's active current consumption varies during the processing of the wake-up signal, and can be found by considering the fraction of time spent in each state and the period of the preamble and bit pattern. Therefore, we can find the active current consumption per wake-up signal by considering equation 5.1.

$$I_{\text{active}} = \frac{t_p}{t_{\text{WuS}}} \cdot I_p + \frac{t_s}{t_{\text{WuS}}} \cdot I_s \quad (5.1)$$

Where t_p and t_s represent the time spent in the processing preamble and processing bit sequence states, respectively. In addition, t_p is equal to the preamble width and t_{WuS} is the period of the WuS. For the proposed address detector, it can be calculated using:

$$t_{\text{WuS}} = t_p + t_s = t_p + g1 + (n \cdot t_{\text{bit}}) + ((n - 1) \cdot g2) \quad (5.2)$$

Where $g1$ and $g2$ are the guard times, t_{bit} is the period of one PWM-modulated bit (assuming the case of an all-one address), and n is the number of bits in the bit sequence.

Figure 5.1.a and Figure 5.1.b show the active state current consumption of the proposed architecture for different WuS parameters, and an address size of 8- and 16-bit, respectively. An additional shift register is required to store the extra bits when processing a 16-bit address, leading to an increase in the processing bit sequence state current as seen in Figure 5.1.b.

The introduction of two operating states within the period of the WuS reduces the value of I_{active} when compared to a two-state detector that processes the same WuS with a constant active current $I_{\text{active}} = I_s$. The proposed architecture achieves varying power savings per WuS depending on the preamble width, bit rate, and address size. For a constant bit rate, the active current consumption is smaller for larger preamble sizes because the detector spends a larger fraction of t_{WuS} in the processing preamble state. On the other hand, the active current consumption increases with increased values of t_{bit} (smaller bit rate) for a constant preamble width. The increase is a result of spending a larger fraction of t_{WuS} in the processing bit sequence state.

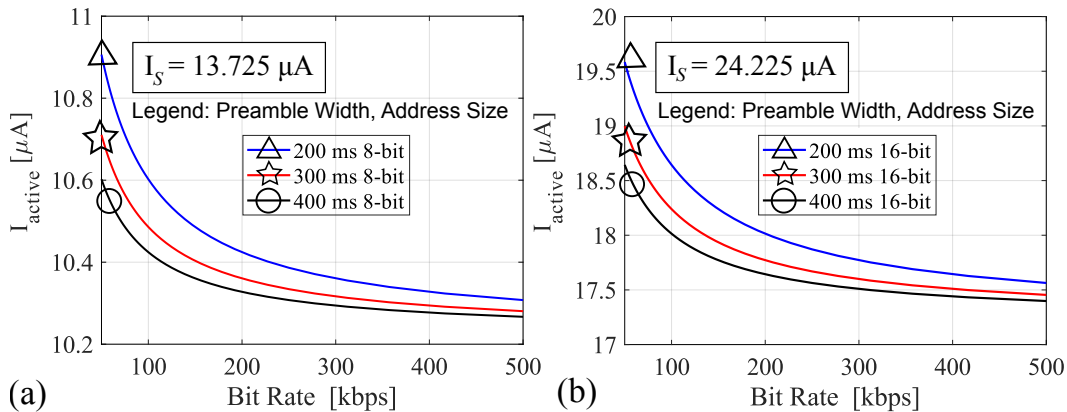


Figure 5.1: Average active current consumption of the proposed detector for different wake-up signal characteristics composed of a. 8-bits and b. 16-bits.

Combined wake-up and charging current consumption

The address detector further reduces its current consumption during charging which is reflected in enhanced power savings when the system receives wake-up and charging signals. To highlight these benefits, we consider a scenario where the system receives one WuS followed by one charging signal. We define I_{combined} as the address detector's average current during a period of one WuS followed by one charging operation. The combined current consumption can be found by considering the fraction of time spent in the charging state (t_c) and the combined charging and wake-up signal period $t_{\text{active}} = t_{\text{WuS}} + t_c = t_p + t_s + t_c$ in Equation 5.1.

We compare the system's combined current consumption with that of a circuit configuration where the PWD remains powered ON during charging operations. This scenario occurs if the RX/harvesting switch is removed from the proposed system (see Figure 4.25). Figure 5.2.a shows the address detector's combined current consumption for different WuS characteristics and charging periods. The combined current decreases for longer charging periods because the detector spends most of the time in the charging state. For a constant charging period and bit rate, the current increases for an increase in the preamble width because the detector spends a smaller fraction of time in the charging state. Further, the decrease in bit rate has a less significant effect on current consumption because t_s is very small compared to t_c . The proposed architecture significantly reduces the circuit's combined average consumption. For example, I_{combined} remains under 0.5 μA for a WuS preamble width of 200 ms followed by a charging signal that lasts for 30 seconds. On the other hand, I_{combined} exceeds 3 μA if the PWD remains powered ON during charging. Similar reduction in I_{combined} is also achieved for different wake-up and charging signal characteristics as shown in Figure 5.2.

5.0.2 Average Current of the Address Detector In a Noisy Environment

In conventional two-state address detectors, the system remains in the listening state if the input power remains below the data slicer's minimum threshold and activates the bit correlator when the data slicer generates a pulse to process the wake-up signal. This method suffers from increased current consumption in noisy environments because the bit correlator is activated whenever the noise level exceeds the system's minimum threshold. On the other hand, the coded preamble concept presented in this work enhances noise immunity because the system moves to the processing preamble state and operates with 25% of its maximum current when the noise level exceeds the minimum threshold. Unlike two-state systems, the bit correlator is only activated when the pulse width is matched.

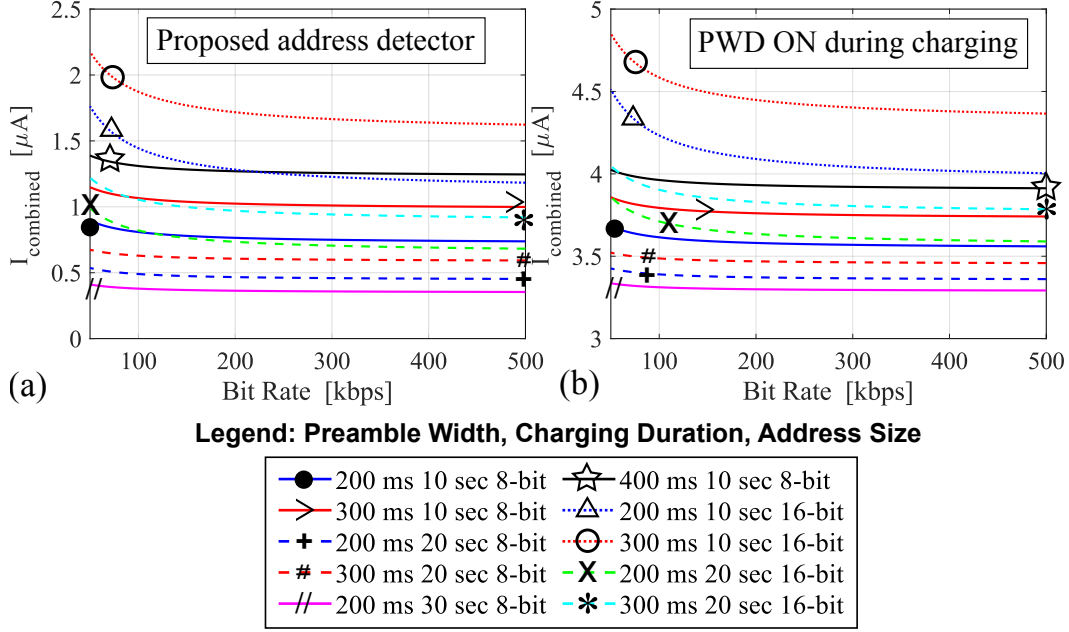


Figure 5.2: Address detector's combined current consumption in operation scenarios involving wake-up and charging. Different plots are shown for a variety of WuS and charging signal characteristics. a. proposed architecture b. No RX/harvesting switching (PWD remains ON during charging).

To highlight the enhanced noise immunity, we consider the average current consumption of the proposed architecture in a noisy environment and compare it to the average current consumption of a two-state detector configuration operating under the same noise conditions. The address detector's average current consumption in a noisy environment can be found using Equation 5.3 and 5.4 for the two-state and multi-power configurations, respectively:

$$I_{\text{noise}} = D_l \cdot I_l \cdot (1 - PF_{\text{threshold}}) + D_s \cdot I_s + D_l \cdot I_s \cdot PF_{\text{threshold}} \quad (5.3)$$

$$I_{\text{noise}} = D_l \cdot I_l \cdot (1 - PF_{\text{threshold}}) + D_l \cdot I_l \cdot (1 - PF_{\text{threshold}} \cdot PF_{\text{preamble}}) + D_p \cdot I_p \cdot (1 - PF_{\text{preamble}}) + D_s \cdot I_s + D_l \cdot I_p \cdot PF_{\text{threshold}} \cdot (1 - PF_{\text{preamble}}) + D_l \cdot I_s \cdot PF_{\text{threshold}} \cdot PF_{\text{preamble}} + D_p \cdot I_s \cdot PF_{\text{preamble}} \quad (5.4)$$

Where D_l , D_p , and D_s represent the fraction of time spent in the listening, processing preamble, and processing bit sequence states, respectively. I_l , I_p , and I_s are the current consumption in each state. $PF_{\text{threshold}}$ is the probability of noise level n exceeding the system's threshold and PF_{preamble} is the probability of false detection of the input noise as a preamble.

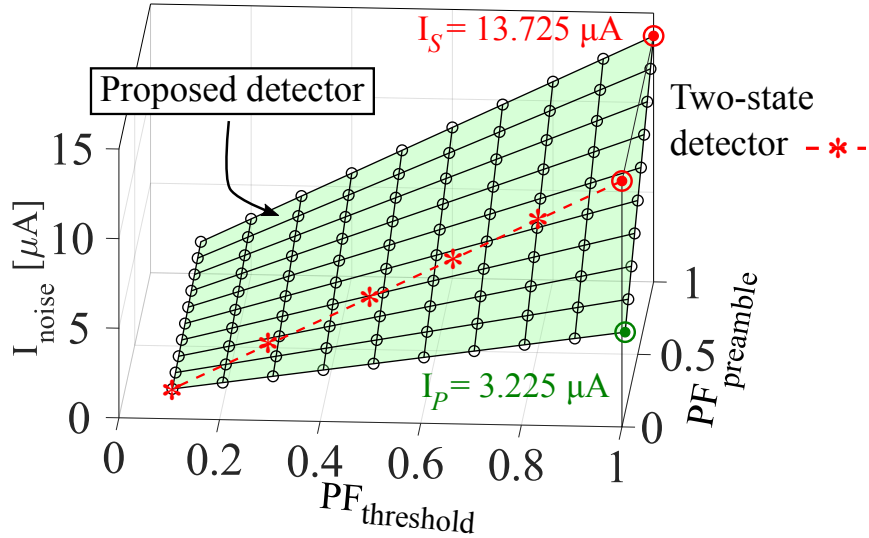


Figure 5.3: Current consumption of the proposed architecture versus a two-state configuration in a noisy environment

The probability of falsely switching from the listening current I_l to the maximum current I_s due to noise is $PF_{\text{threshold}}$ for the two-state detector and $PF_{\text{threshold}} \cdot PF_{\text{preamble}}$ for the multi-state address detector. Therefore, the increase in noise level causes an increase in current consumption for both configurations; however, the proposed address detector has a smaller current consumption for the same noise power when $PF_{\text{preamble}} < 1$. Figure 5.3 shows the average current consumption for the two-state and multi-state detectors. At the maximum noise level ($PF_{\text{threshold}} = 1$), the two-state address detector operates at the maximum current of I_s , while the multi-power address detector remains in the processing preamble state. Its current reaches I_s when the preamble is falsely detected. Based on the experimental results and analytical discussion, we conclude that the coded preamble scheme leads to three benefits: 1) Preamble can be used for addressing. 2) Reduced active current consumption per WuS. 3) Enhanced noise immunity.

5.0.3 Average Current Consumption and Lifetime of the IoT Device

RF wake-up allows IoT to operate on-demand and extend their lifetime. To find the average current consumption of the IoT device, we consider the probability of false state change as in the previous section. An additional probability, the probability of false trigger, is considered when the bit correlator generates a false wake-up trigger to the device. We define the probability of false wake-up when using the multi-power-address detector as follows:

$$PF_{\text{Wake-up}} = PF_{\text{threshold}} \cdot PF_{\text{preamble}} \cdot PF_{\text{sequence}} \quad (5.5)$$

Where PF_{sequence} is the probability of false detection of the bit sequence by the bit correlator. The average current consumption of the device is determined by D_{ON} and $(1 - D_{\text{ON}})$, the fraction of time spent in sleep and active modes, respectively. It can be calculated using equation 5.6:

$$I_{\text{avg,IoT}} = D_{\text{ON}} \cdot I_{\text{ON}} + (1 - D_{\text{ON}}) \cdot I_{\text{ON}} \cdot PF_{\text{Wake-up}} + (1 - D_{\text{ON}}) \cdot (1 - PF_{\text{Wake-up}}) \cdot I_{\text{sleep}} \quad (5.6)$$

We consider the Libelium Sensor used in Chapter for 4 to assess the average current consumption and lifetime of a typical IoT unit when integrated with the multi-power address detector.

Figure 5.4 shows average current consumption of the Libelium unit with $I_{\text{ON}} = 367.8$ mA, $I_{\text{Sleep}} = 0.833$ mA, and $C = 3200$ mAh [5] for different values of partial false wake-up probabilities and a wake-up period 1 hour. The multi-stage activation of the different address detector units keeps $PF_{\text{Wake-up}}$ small and significantly increases the lifetime of the device. For example, the average current consumption remains below 100 μA for $PF_{\text{Trigger}} = 0.2$. We can also assume that $PF_{\text{threshold}} > PF_{\text{preamble}} > PF_{\text{sequence}}$ because the more advanced power states are responsible for examining more complex attributes of the WuS. For instance, PF_{preamble} describes the probability of noise exceeding the system's minimum threshold. On the other hand, PF_{sequence} describes the probability of receiving an erroneous bit sequence. Therefore, the cascaded architecture of the multi-state address detector reduces the false wake-up probability by multiplying the different partial probabilities. The increase in complexity of the addressing scheme leads to increased complexity of the address detector circuit, but reduces the probability of false wake-up of the device. The increase of power consumption of the address detector is compensated by introducing the multiple power consumption states.

The lifetime of the IoT device is determined by the noise immunity of the wake-up receiver, as shown in Figure 5.5. A special case is seen in Figure 5.5.d where $PF_{\text{sequence}} = 1$ indicating that the device is triggered when the preamble is matched, regardless of the following bit sequence. The average lifetime of the IoT device is extended by implementing the bit sequence in the addressing scheme at the expense of decreased lifetime of the address detector due to the increase in the current consumption required to process the bit sequence.

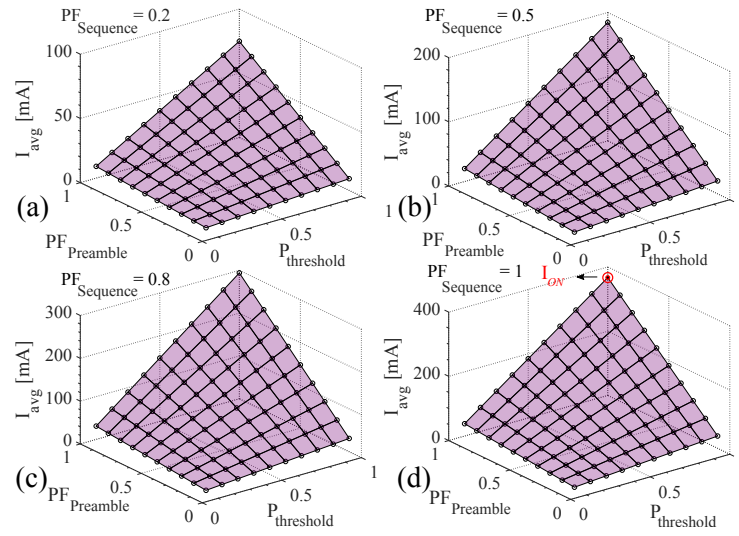


Figure 5.4: Average current consumption of an IoT device in a noisy environment.

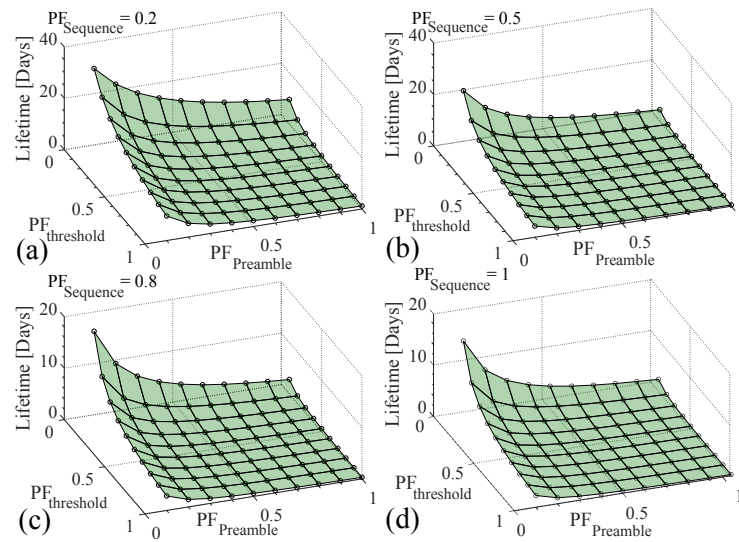


Figure 5.5: Average lifetime of an IoT device in a noisy environment.

Chapter 6

Power Management System

Combined RF energy harvesting and wake-up offers IoT devices maximum energy savings and enhanced autonomy. The energy available at the output of the rectifier can be stored and serve as an energy source for active components such as the address detector or an IoT device. Before delivering the harvested energy to the device, it needs to be stored and regulated by a power and management unit (PMU). In this Chapter, we propose a PMU design to integrate with the address detector proposed in Chapter 4 and 5. The main objective when designing the PMU is to achieve passive boost and regulation of the rectified voltage at the lowest possible input power level. The combined energy harvesting and wake-up system is shown in Figure 6.1. The same antenna and rectifier are used to charge the energy storage and to receive and process the wake-up signal. The harvesting system is fully passive and always operational. It boosts and stores the input DC voltage into a storage element when the received signal power level (P_r) exceeds the minimum threshold. An advantage of combining harvesting and wake-up functionalities is that the harvesting system charges the energy storage while the wake-up signal is received. Therefore, wake-up signals with a slower bit rate allow more time to charge the energy storage, but increase wake-up delay.

The harvested energy is delivered to active components through a regulator to protect the circuit from sudden spikes or a drop in the harvested energy. The system might have an additional battery to provide power in the event the harvested energy is not adequate. When connecting a PMU at the output of the rectifier, a DC loading effect exists as shown in Figure 6.2. The voltage supplied to the PMU, represented as R_L is a function of the input resistance looking into the rectifier (R_i) and the input resistance of the PMU (R_0). The value G represents the gain of the system. In this case it represents a negative gain to model the losses occurring between the output of the rectifier and the PMU and parasitic effects of the PMU. It is crucial to have good impedance matching between the rectifier and the PMU to maximize the power transfer and eliminate loading effects. In addition, the

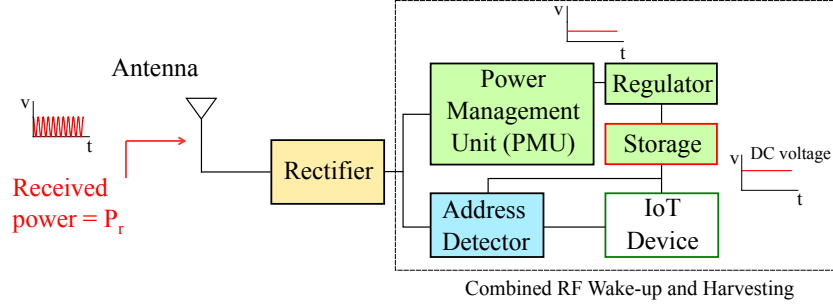


Figure 6.1: Block diagram of a combined RF harvesting and wake-up system

rectifier must be capable of inputting a current large enough for the PMU to operate. The values of the series resistances R_S and R_O must be small for the rectifier DC voltage V_S to appear across R_L .

6.1 Single Stage and Double-Stage Voltage Regulator

A passive voltage regulator is designed and tested to boost and regulate the output voltage of the rectifier. The designed regulator is characterized with a minimal quiescent current and does not require an active bias source to operate. We present the voltage regulator in two variants for different applications:

1. Single-stage passive voltage regulator at 3.3 V
2. Double-stage passive voltage regulator at 4.4 V

6.1.1 Single-stage passive voltage regulator

The single stage voltage regulator is shown in Figure 6.3. It is composed of a single TPS610982 chip [78] containing one boost and one low-dropout regulator outputs and it is configured to operate in low power mode. The chip boosts and regulates the input signal, and the DC boosted voltage (3.3 V) appears at the VMAIN pin and is used to power an IoT device (or the address detector). The (LDO) output (2.8 V) appears at the VSUB pin. The regulator delivers stable voltage at the two outputs for input voltages that exceed the minimum threshold. On the other hand, the input voltage is delivered directly to the output when the input voltage exceeds the higher threshold. Table 6.1 shows the parameters of the single-stage regulator. It has a quiescent current consumption of 300 nA and can boost an input voltage as low as 700 mV.

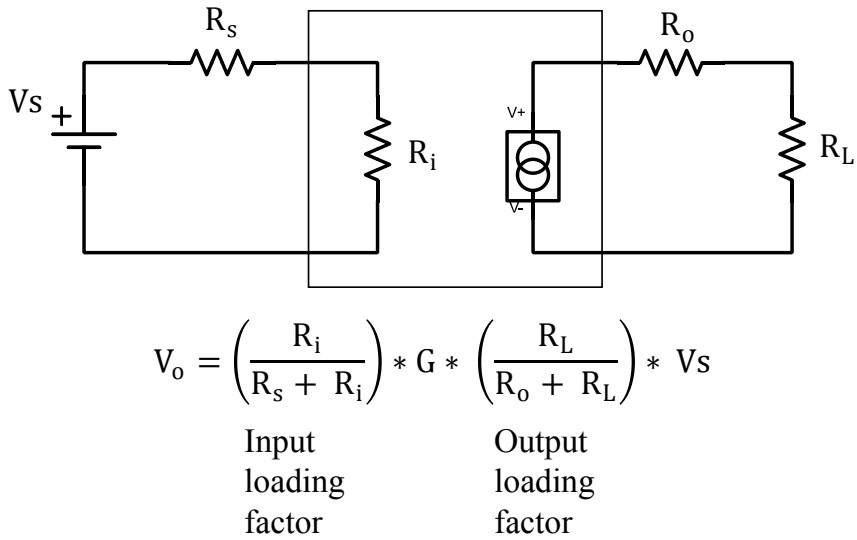


Figure 6.2: DC loading effect affects between the rectifier, represented by a voltage source, and the PMU, represented by a load. V_S represents the rectifier output voltage and G represents the system's gain.

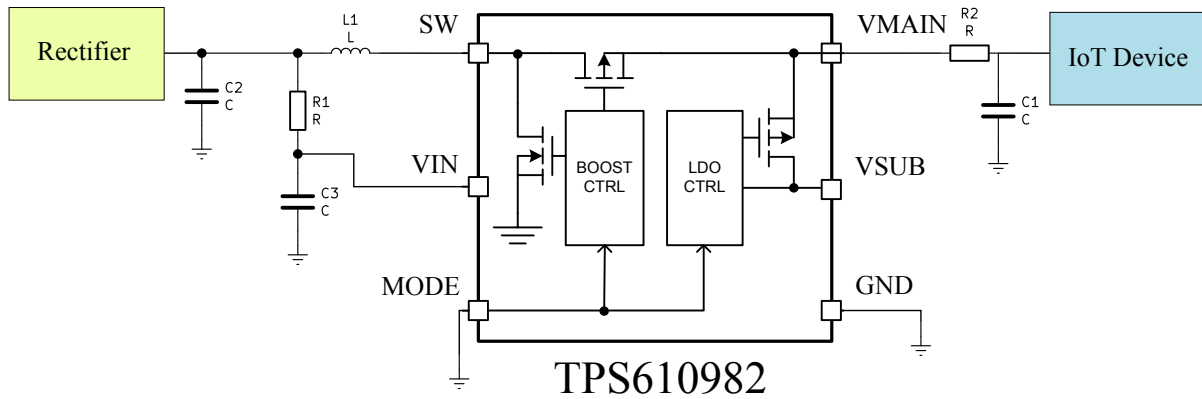


Figure 6.3: Single-stage regulator configuration

6.1.2 Double-stage passive voltage regulator

A double-stage passive voltage regulator is designed for applications that require a higher output voltage. The double stage voltage regulator circuit is shown in Figure 6.4. We use a single-stage regulator to boost the input voltage to 3.3 V at the output of the DC-DC boost. This output is connected to the input of

Table 6.1: Single-Stage Regulator Parameters

| Parameter | Value |
|-------------------------------|--------------|
| Quiescent current consumption | 300 nA |
| Minimum input voltage | 700 mV |
| Boost output | 3.3 V |
| LDO output | 2.8 V |
| Max. output current | 50 mA |

the second stage that comprises a TPS610987 voltage regulator [78] operating in active mode. The LDO output of the first stage (2.8 V) is connected to the MODE pin of the second stage to set its operation in active mode. Table 6.2 shows the parameters of the double-stage regulator. The quiescent current consumption remains the same (300 nA) because only the first stage draws current from the rectifier.

Table 6.2: Single-Stage Regulator Parameters

| Parameter | Value |
|-------------------------------|--------------|
| Quiescent current consumption | 300 nA |
| Minimum input voltage | 700 mV |
| Boost output | 4.3 V |
| LDO output | 3.1 V |
| Max. output current | 50 mA |

6.1.3 Voltage Regulators Fabrication and Testing

The single- and double-stage regulators were fabricated on an FR4 substrate and tested for a dedicated input voltage (DC power supply) and a rectifier. The fabricated designs are shown in Figure 6.5. Table 6.3 shows a list of values of the lumped elements and their part numbers if a specific vendor is required for proper operation.

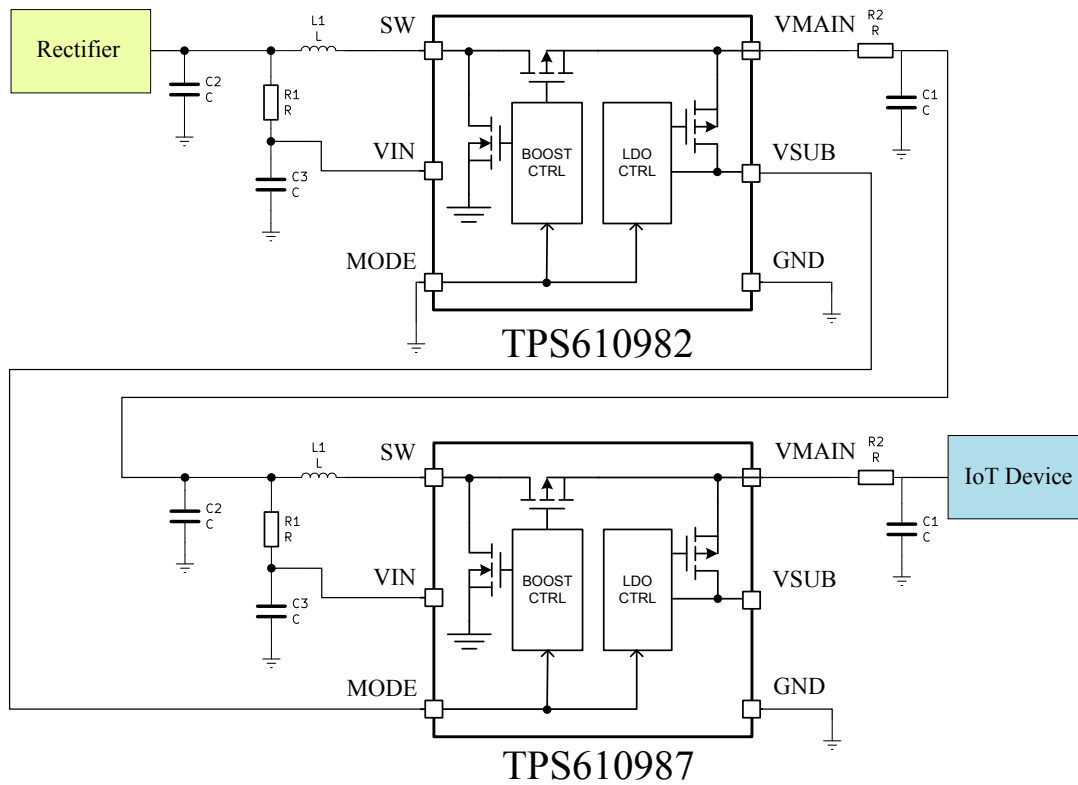


Figure 6.4: Double-stage regulator configuration

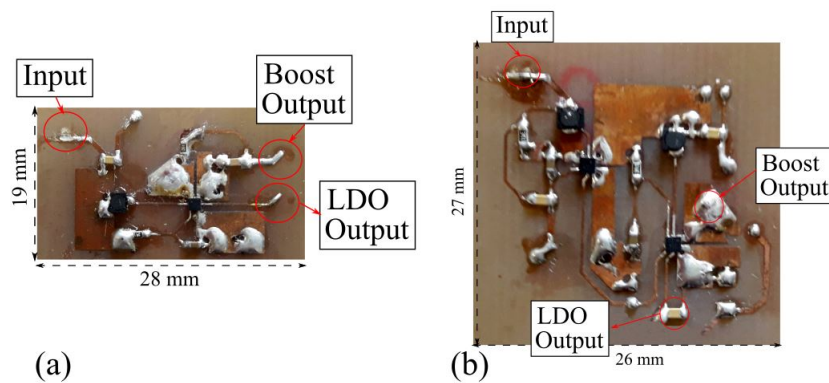


Figure 6.5: Fabricated regulator circuit. a) Single-stage regulator. b) Double-stage regulator

Table 6.3: Double-Stage Regulator Parameters

| Components Name | Value |
|-----------------|------------------|
| R1 | 390 Ω |
| L1 | 47 μH |
| C2 | 10 μF |
| C3 | 1 μF |
| C1 | 1 μF |
| R2 | 100 k Ω |

The single- and double-stage regulators deliver a regulated voltage of 3.3 V and 4.3 V, respectively when tested with a DC voltage supply. However, when tested with a rectifier, the VMAIN output remains OFF. We conclude that the low input impedance of the TPS310982 chip is causing a DC loading effect issue when connected to the rectifier. Therefore a power management unit with a maximum power point tracking mechanism is introduced to boost the input voltage from the rectifier.

6.2 Power Management Unit

A BQ25570 Power Management Unit [79] is implemented to boost and regulate the output DC voltage of the rectifier into a storage element, as shown in Figure 6.6. The PMU is composed of passive components and does not require a biasing source. It regularly samples the input rectifier's DC voltage through the voltage divider formed by ROC1 and ROC2. Its input impedance is varied to ensure maximum power transfer from the rectifier to the storage element. A sampled reference voltage is maintained across CREF.

The PMU contains a boost charger which steps up the input voltage. When starting from an empty capacitor, the PMU requires an input DC voltage of 600 mV to charge CSTOR on the VSTOR pin (cold start operation). Once the voltage across the CSTOR reaches $V_{th} = 1.8$ V the main boost charger is turned on, and the storage capacitor is charged to the value determined through resistor R11. The output voltage is tuned to 4.5 V by setting the VBAT_OV pin through the voltage divider of ROV2 and ROV1. When the VSTOR voltage exceeds the threshold, VRDIV is turned on every 64 ms to provide a bias source for different voltage dividers in the circuit, leading to a reduction in power consumption.

The PMU has a quiescent current consumption of 488 nA and appears as a high impedance connected in parallel with the rectifier's diode. Therefore, the PMU

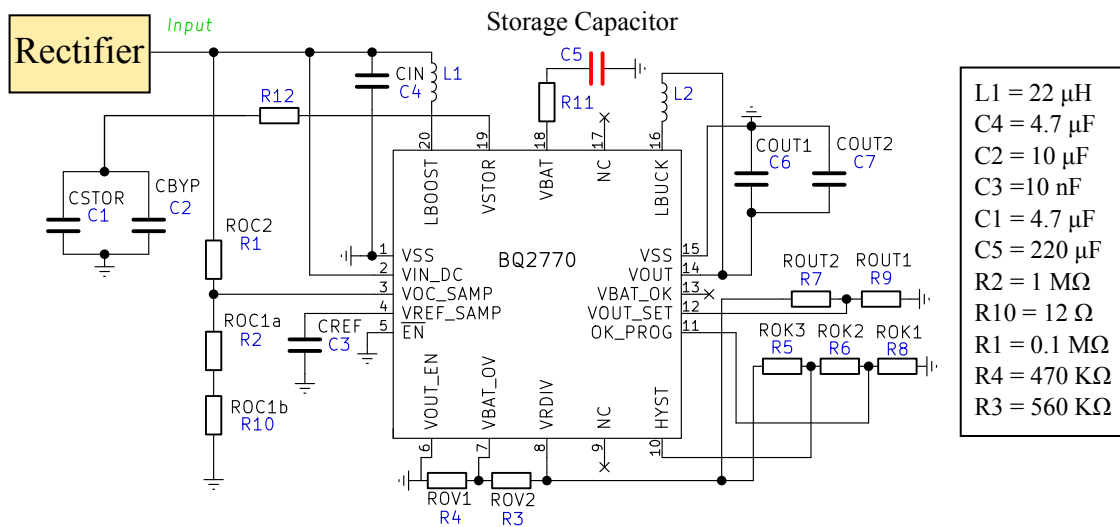


Figure 6.6: Power management unit (PMU) circuit

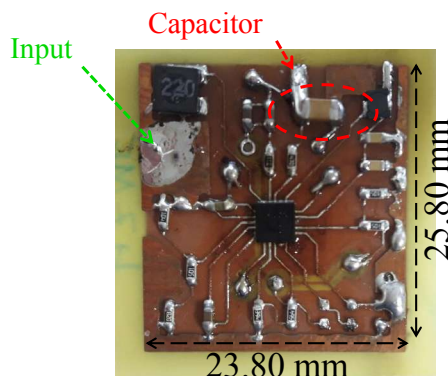


Figure 6.7: Fabricated power management unit circuit

input DC voltage is approximately equal to the rectifier’s open-circuit voltage.

6.2.1 Power Management Unit Fabrication and Testing

The designed power management unit is fabricated on an FR4 substrate and has dimensions of 23.8 mm x 25.8 mm and is shown in Figure 6.7. The figure also shows the values of the lumped component used to to configure the PMU.

The power management unit operation is verified for received power of 0 dBm at the input of the rectifier, and the results are shown in Figure 6.8. Figure 6.8(a) exhibits charging an empty 220 μF storage capacitor from a cold start state ($V_{STOR} \leq V_{th} = 1.8$ V), where V_{th} is the threshold voltage required to initiate the

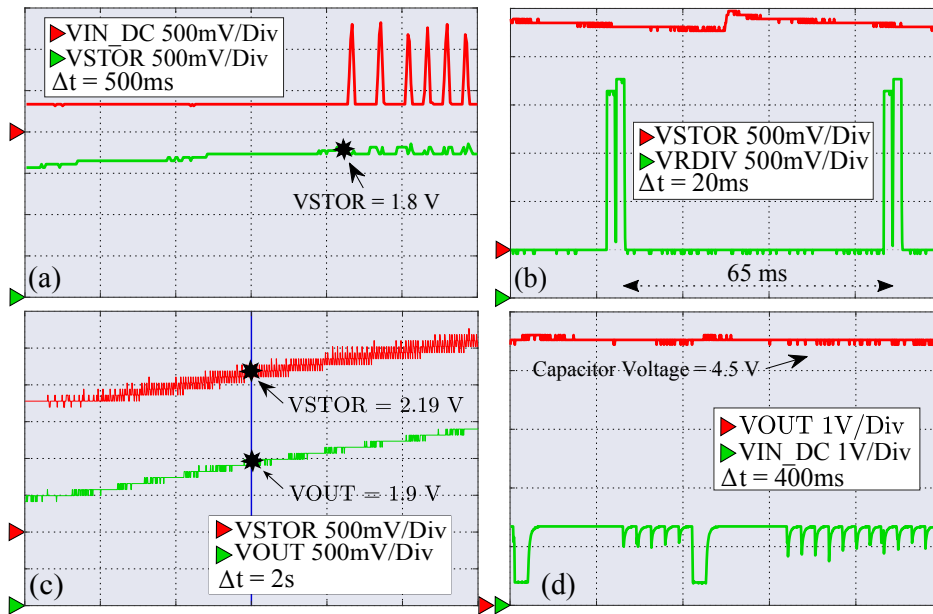


Figure 6.8: Charging at $P_r = 0$ dBm. (a) Initializing the main boost charger. (b) Periodically turning on VRDIV to provide bias. (c) VOUT is slightly lagging the voltage at the temporary storage. (d) Stabilizing VOUT at 4.5 V

main boost charger. The main boost charger continues to raise the input voltage until it reaches the tuned output value of 4.5 V. Figure 6.8(b) shows the power management unit activating the primary biasing source at the VRDIV pin for a short period every 65 ms to provide biasing for the entire circuit and reduce current consumption. Figure 6.8(c) shows an increasing voltage of the storage capacitor and the voltage at the temporary storage capacitor (CSTOR). The temporary storage capacitor voltage is slightly larger than the primary storage voltage. Finally, Figure 6.8(d) shows the main storage capacitor's voltage stabilizing at 4.5 V.

Chapter 7

Leveraging UAVs for RF Wake-up and Charging

In this Chapter, we implement the address detector and power management system that we developed in Chapter 4 and Chapter 5 in a combined harvesting and wake-up system that shares the same antenna and rectifier for UAV-enabled RF energy harvesting and wake-up. The main objective of this work is to demonstrate the feasibility of using a UAV in an agricultural application where sensors are scattered on the ground to perform different functions, such as applying fertilizers, measuring environmental variables, and controlling irrigation.

It was shown in [1] that using IoT technology can be useful to track plants' growth and optimize irrigation. The implemented system, however, is limited to small areas, and extending the solution requires the addition of a Wi-Fi transceiver to communicate with the different sensors. In an application where this solution is used to monitor large greenhouses or agricultural fields, sensors and main transceivers can be put to sleep mode to reduce their current consumption, and a UAV can be dispatched to leverage its high mobility to charge the batteries and trigger sensors to operate. Therefore, in this chapter, we study the technical specifications of such a system, and we examine the limitations on using the UAV to facilitate large scale smart agricultural solutions.

The proposed ground unit stores energy from the low input power signal of the UAV. In addition, the address detector is used to receive a targeted wake-up signal from the UAV and trigger an IoT device in an agricultural application. We provide an experimental testbed of using a UAV for combined RF harvesting and wake-up, and study its different parameters, such as sensitivity, range, wake-up selectivity, and charging time.

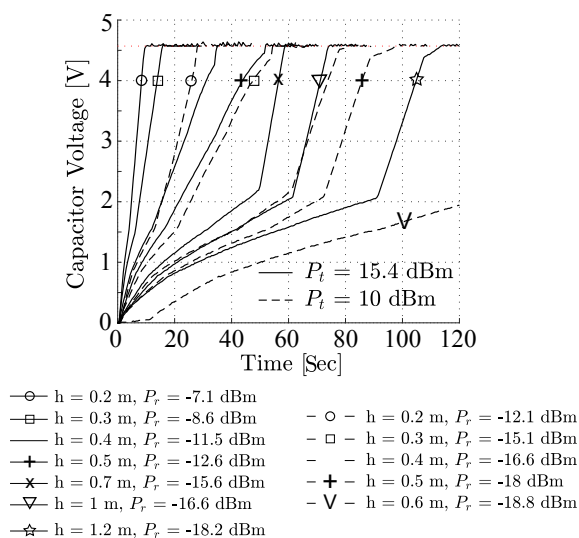


Figure 7.1: Capacitor charging time at a variable UAV height using 12.6 dBi antenna

7.1 UAV RF Harvesting Results

In this experiment, a passive RF energy harvesting system is placed on the ground, and a UAV equipped with an RF transmitter is used as a source of a 2.4 GHz continuous signal to charge a 120 μF storage capacitor from cold start to a regulated voltage of 4.5 V. The main objective of the experiment is to find the capacitor charging time for different UAV heights above the ground, i.e. the maximum height at which the capacitor can be charged using the UAV. The UAV and the harvester are equipped with a 2×1 meandered antenna array with a maximum gain of 12.6 dBi [55]. The received signal power is measured, and the voltage curve is plotted across the storage capacitor while the height is varied.

The resulting voltage curves, presented in Figure 7.1, show that a slight increase in height leads to a significant increase in the time required to charge the capacitor. The minimum required received power for charging an empty storage capacitor is found to be -18.2 dBm at the receiver's antenna. Furthermore, the maximum achieved charging distance is 0.5 m at a transmit power of 10 dBm. The maximum range can be increased to 1.2 m by increasing the transmit power to 15.4 dBm, however, increasing the transmit power level should be carefully considered because it leads to a faster drain of the UAV's battery. The operation time of the UAV is determined by the capacity of the battery that powers the transmitter and the weight of the payload. With a payload composed of the transmitter that is powered by a single-cell (3.7 V) LiPo battery with a capacity of 2000 mAh (450 grams), the flight time of the UAV is around 12 minutes at a velocity of 40 km/h.

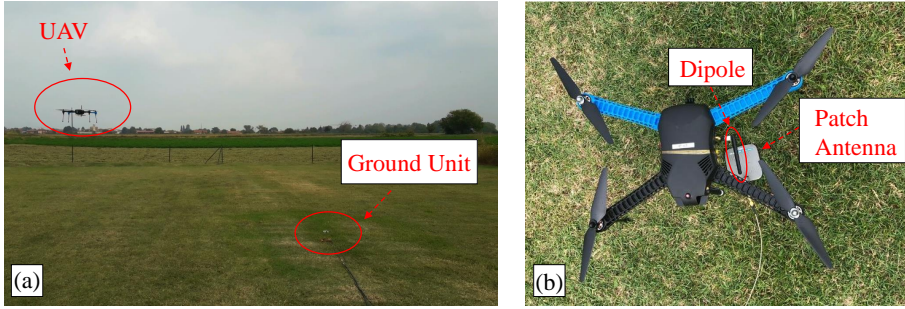


Figure 7.2: Employing a UAV for RF charging and wake-up of sensors

To demonstrate the ability to perform harvesting without the need for dedicated high-gain antennas, we employ commercially available antennas for both UAV and harvesting unit. The transmitter power (transmitter 5015 from Valon Technology) is set to 15 dBm. The UAV is equipped with a 3 dBi dipole antenna and the IoT device is equipped with a 6 dBi patch antenna. The UAV lands on top of the ground unit to charge the capacitor as shown in Figure 7.2.

The maximum height at which the capacitor can be charged to 4.5 V is found to be 20 cm as seen in Figure 7.3. The figure shows the voltage curves obtained when the UAV lands with different distances between the UAV’s dipole antenna and the harvester’s patch antenna. During the experiment, the UAV becomes more prone to ground effects [80] when it gets in close proximity to the harvester on the ground, which can be detrimental to its ability to land precisely on the harvester. Figure 7.3 shows the voltage curve when the UAV lands with an offset d of 10 cm on the horizontal plane with a height h of 10 cm. It can be seen that the charging time is a function of the diagonal distance.

7.2 UAV RF Wake-up Results

An experiment comprising the dual-mode ultra- low-power PWD developed in Chapter 4 is conducted to test UAV-based RF wake-up and demonstrate wake-up selectivity. Two PWD units are fabricated with each tuned to a different pulse width. The values of the tuning resistors (R_1 and R_2) are set to 330 k Ω and 270 k Ω for address detector (A). As for address detector (B), they are set to 356 k Ω and 330 k Ω , respectively.

Figure 7.4 shows the output of the two detector circuits when a modulated wake-up signal is received by both detectors at a power of -18.2 dBm. A wake-up signal is received between t_1 and t_2 . Only a received signal with a width 3000 ms leads to triggering detector (A) at time t_3 . Whereas for detector (B), this value is set to 4000 ms. The auto power-off circuit disconnects the power supply from the

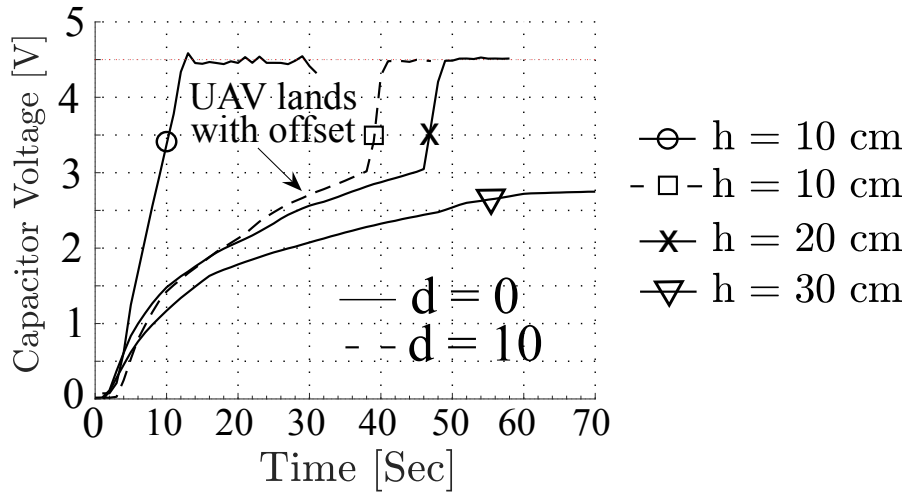


Figure 7.3: Capacitor charging time using a 3 dBi dipole antenna and a 6 dBi patch antenna

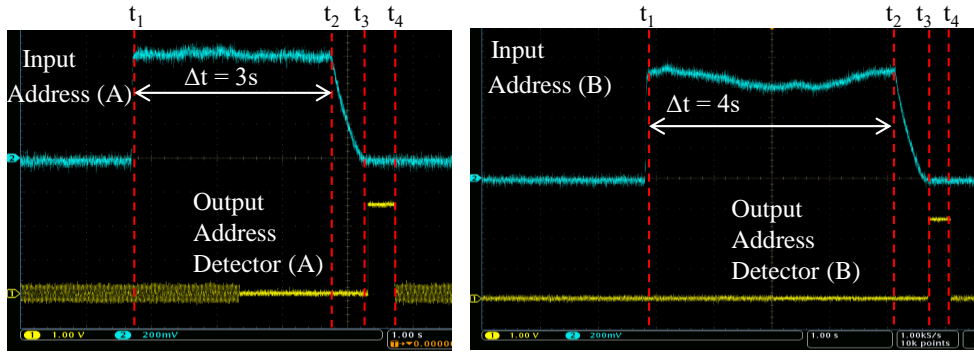


Figure 7.4: Demodulation of received signal and selective wake-up of sensors

address detector at time t_4 to reduce its power consumption.

The wake-up event triggered by the UAV is captured in Figure 7.5. The UAV hovers at a height of 2 meters over the IoT device as shown in Figure 7.2(a) and repeatedly transmits wake-up signals with a transmit power of 10 dBm. Figure 7.5 shows the output of address detector (A) when a modulated signal with an input power of -15.2 dBm is received from the UAV. In order to find the wake-up sensitivity, the distance between the transmitter and receiver is increased in an outdoor environment and repeated wake-up signals are transmitted. The wake-up sensitivity is found to be -40 dBm with a wake-up range of 27.5 m at a transmit power of 15.4 dBm. The obtained wake-up range shows good agreement with the calculated value of 30 m using using a standard line of sight path loss model.

A summary of the obtained results for the UAV RF harvesting and wake-up experiments are shown in Table 7.1 for a transmit power of 15.4 dBm and an antenna gain of 12.6 dBi. The distinctive feature of the proposed system is com-

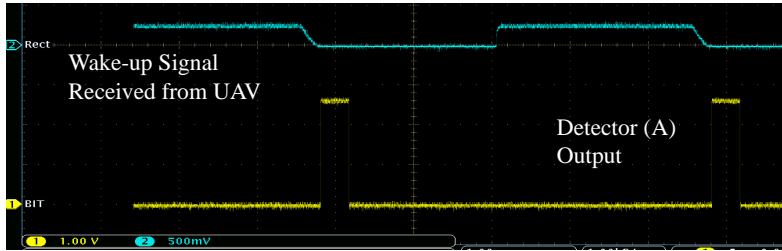


Figure 7.5: Receiving a wake-up signal from a UAV

Table 7.1: Summary of Obtained Results

| Scenario | Sensitivity | Consumption | Range | Delay |
|-------------------|-------------|-------------|--------|-------|
| Harvesting | -18.2 dBm | Passive | 1.2 m | 120s |
| Wake-up | -40 dBm | 8.2 μ W | 27.5 m | 4s |

bined passive RF harvesting/ultra-low-power wake-up with outstanding sensitivity. Moreover, the UAV can hover at high altitudes to wake-up a specific sensor, or decrease its altitude to charge the sensor’s battery.

By considering the experimental results, we can see that the UAV can cover areas of 25 m² while hovering at a height of 5 m. Typical greenhouses can have an area of around 267 m². Therefore, the mobility of the UAV is particularly beneficial to provide full coverage of agricultural greenhouses. On the other hand, the coverage area for harvesting decreases due to limitations of sensitivity. Nevertheless, our experimental results show that the UAV can still charge an energy storage on the ground while still hovering with an altitude that is high enough to avoid colliding with vegetation. However, further work can be done in the future to study the effect of obstacles on charging in agricultural applications. The study in [81] shows that the use of the path loss model is limited for charging applications with dense vegetation even if the distance is small. The authors propose a channel model which takes into consideration different parameters related to agricultural applications, such as plant height and density.

Chapter 8

Comparison and Conclusion

8.0.1 Comparison with State-of-the-Art

In this section, we provide a comparison between this work and similar efforts reported in the literature. The available designs are implemented using discrete, off-the-shelf components, or through CMOS fabrication, as shown in Table 8.0.1. Our approach uses discrete components and offers a low current consumption, fast bit rate, and supports combined charging and wake-up with a minimal current consumption during charging.

Examples of hardware realized through discrete components are found in [3, 39, 40]. A microcontroller is used as a bit correlator in [3] and [39]. The design in [3] implements a passive noise rejection preamble, and a preamble composed of one Return-to-Zero (RZ) encoded 1-bit is used in [39]. On the other hand, the AS3933 [82] correlator used in [40] offers a low active current consumption of 8 μA , a sensitivity of -52 dBm, and a bit rate of 1 kbps.

Various designs are realized using CMOS technology to achieve a compact size and enhanced performance. Higher sensitivity is achieved by implementing an RF amplification stage at the expense of higher current consumption [31] [23] [28] [83] [84]. The method in [83] achieves the highest sensitivity in this comparison. It is obtained at a constant current consumption of 123 μA and a data rate of 10 kbps. While some CMOS designs achieve a higher sensitivity when compared to our work, it is important to note that our approach does not include an active RF amplification stage which decreases our system's complexity and current consumption [31] [23] [28] [83] [84].

A current consumption in the few- or sub-microamp range is reported in [30] [52] [41]. The design in [41] also features PWM modulation and clock extraction. It achieves a current consumption of 1.8 μA and a bit rate of 80 kbps. The design in [52] also offers clock extraction using Manchester Coding. The circuit exhibits a constant current consumption of 2.3 μA during listening and processing states, and

a sensitivity of -47 dBm. The authors in [30] achieve a current consumption of 11.25 nA and a bit rate of 0.3 kbps. The design includes a passive RF amplification stage and has a sensitivity of -69 dBm.

Table 8.1: State-Of-The-Art Comparison

| Design | Tech. | Combined Harvest/Wake-up | Freq. | Modulation Scheme | Sensitivity [dBm] | Clocking Source | Bias [V] | Bit Rate [kbps] | Preamble Function | Current Consump. (listening) [μ A] | Current Consump. (active) [μ A] | Current Consump. (Charging) [μ A] |
|-----------|--------------------|--------------------------|-------------|-------------------|-------------------------|----------------------|----------|----------------------|-------------------|---|--------------------------------------|--|
| This Work | Discrete-Component | Yes | 2.42 GHz | PWM | -40 | Extracted From Input | 2.6 | 500 | Addressing | 0.225 | 3.225; 13.725 ¹ | 0.15 |
| [3] | Discrete-Component | No | 868 MHz | OOK | -32 | pC | 1.8 | 10 | Noise Filtering | 0.106 | 35 | NA |
| [39] | Discrete-Component | Yes | 915 MHz | OOK | SEE NOTE 2 | pC | 2.2 | 33.3 | Noise Filtering | 0.13 | 270 @ 1 MHz | 0.13 |
| [40] | Discrete-Component | No | 2.4 GHz | OOK ³ | -52 | AS9933 [82] | 3 | 1 | Sync. | 3.6 | 8 | NA |
| [28] | CMOS | No | 902-928 MHz | OOK | -78.5; -75 ⁴ | Local Osc. | Variable | 10; 200 ⁵ | Sync. | 16.4 ⁶ | 22.9 ⁶ | NA |
| [41] | CMOS | No | 433.9 MHz | PWM | -30 ⁷ | Extracted From Input | 1.5 | 80 | Noise Filtering | 0.28 ⁸ | 1.8 | NA |
| [31] | CMOS | No | 45 MHz | FSK | -62.7 | Local Osc. | 0.7 | 200 | NA | 53.5 | 53.5 | NA |
| [83] | CMOS | No | 780-950 MHz | OOK | -86 | Extracted From Input | 1 | 10 | NA | 123 | 123 | NA |
| [84] | CMOS | No | 80 MHz | FSK | -62 | Local Osc. | 0.7 | 312 | NA | 64.2 | 64.2 | NA |
| [52] | CMOS | No | 2.45 GHz | OOK | -47 | Extracted From Input | 1 | 200 | Sync. | 2.3 | 2.3 | NA |
| [23] | CMOS | No | 2.4 GHz | OFDM ⁹ | -72 | Local Osc. | 0.95 | 62.5 | Sync. | 121 | 182 | NA |
| [30] | CMOS | No | 113.5 MHz | OOK | -69 | Local Osc. | 0.4 | 0.3 | NA | 0.01125 | 0.01125 | NA |

¹ Sensitivity is not reported in dBm. The wake-up range is 1.16 m with 13 dBm transmit power. ² Subcarrier modulation of 2.4 GHz signal emulating an OOK signal. ³ -78.5 dBm and -75 dBm in listening and detection modes, respectively. ⁴ 10 kbps and 200 kbps in listening and active modes, respectively. ⁵ -30 dBm for a bit rate of 80 kbps ⁶ 180 nA for the address detector + 100 nA for the microcontroller. ⁷ OOK emulating OFDM. ⁸ 3.225 μ A (processing preamble); 13.725 μ A (processing bit sequence).

8.0.2 Conclusions and Future Work

In this thesis report, an address detector for systems employing combined wake-up and charging is introduced. To minimize our architecture's current consumption, a multi-power approach is suggested where the circuit continuously spins between different states, consuming a varying current. The circuit senses the input received from the rectifier and determines the next action to take (switch ON a complex bit correlator, return to listening, or turn off the main circuitry while the device is charging). The preamble's role is extended beyond simple noise filtering by encoding a message in its varying width. The hardware shows flexibility in detecting the coded preamble and the following PWM-modulated bit pattern. It can be tuned to identify pulses with a width ranging from a few hundred microseconds to a few milliseconds by adjusting a variable resistor and delivers a maximum data rate of 500 kbps. The proposed detector offers a minimal current consumption of 0.225 nA by shutting down its main components. In addition, the multi-power approach leads to reduced active current consumption, ability to charge faster and from lower power levels, and enhanced noise immunity.

The designed system is tested for agricultural applications by considering a scenario to wake-up a wireless sensor using commercial routers. The wake-up system can be implemented using commercial Wi-Fi routers without modifying their hardware or software. Therefore, it is easy to implement in agricultural greenhouses with a pre-existing Wi-Fi infrastructure. Furthermore, we tested the feasibility of using a UAV as a transmitter for harvesting and wake-up applications to provide coverage to agricultural fields with devices scattered on the ground to perform different functions. Although our experimental results were limited to using a watermark sensor, the proposed system can leverage a variety of applications which rely on leaf moisture, chemical, wind, light, or wind sensors. By harvesting radio signals, we can avoid the tedious task of battery replacement. Furthermore, the wake-up functionality allows us to power OFF the transceivers of sensors which use Wi-Fi technology to relay measurements.

The main challenge in designing wake-up receivers is enhancing noise immunity while ensuring a small current consumption. In the proposed design, noise immunity is enhanced by introducing the multiple operation states and the coded preamble. However, the designed system's noise immunity can be further improved to avoid jamming and excessive switching between the different states in noisy conditions. Moreover, the wake-up integrity can be improved to avoid unwanted wake-ups which can drain the battery or compromise security. The concept of IoT hardware designs for enhanced security has recently gained attention as a way to secure IoT networks while maintaining a small current consumption [85]. Secure RF WuRx hardware architectures may extend the applications of RF wake-up to sensitive areas such as biomedical devices.

Extending the harvesting range while ensuring passive operation is another future challenge to address to enhance the operation of combined harvesting and wake-up systems. In this work, the maximum reported distance for reliable wake-up is 27.5 meters, while for harvesting it is limited to 1.2 meters, using the same transmit power and antennas for both tasks. The limitation for the harvesting range stems from the requirement to rely on a passive harvesting system and the low sensitivity of the PMU, which is limited to 700 mV. A possible solution to this issue can be found by considering an intermediate boost stage between the rectifier and the PMU that is characterized by a higher sensitivity. In addition, it is possible to consider co-designing the rectifier and PMU to optimize efficiency and enhance the rectifier's output voltage.

Backscattering communications can be implemented at the receiver to reduce the current consumption of the IoT device. The RF transmitter is the component with the highest current consumption in any communication system. For example, the IoT sensor board used in this work is equipped with a Wi-Fi module with a current consumption of 367 mA. This value is significantly greater than the current consumption required for sensing, which is limited to a few milliamps. Sensor data can be used as a digital signal to modulate the antenna's impedance matching, thus allowing the receiver to switch between reflection and reception to perform backscattering. A possible challenge in integrating backscattering sensor data transmission with the proposed system is switching between the operation modes of receiving, charging, and transmitting (backscattering). In addition, it is difficult to isolate the three modes because they operate at different power levels. Nevertheless, the significant power savings gained from relying on backscattering encourages further work in this area. The improvements gained from our approach, in addition to further enhancements such as backscattering make the design suitable for applications that rely on harvesting and wake-up to minimize power consumption and extend battery life.

Appendix A

Abbreviations

| | |
|------|--|
| RF | Radio Frequency |
| IoT | Internet of Things |
| PMU | Power Management Unit |
| WuTX | Wake-up Transmitter |
| WuS | Wake-up Signal |
| WuRX | Wake-up Receiver |
| WSNs | Wireless Sensor Networks |
| PWM | Pulse Width Modulation |
| OOK | On-Off Keying |
| LNA | Low-Noise Amplifier |
| OFDM | Orthogonal Frequency Division Multiplexing |
| ASK | Amplitude-Shift Keying |
| FSK | Frequency-Shift Keying |
| PSK | Phase-Shift Keying |
| PWM | Pulse Width Detector |
| UAV | Unmanned Aerial Vehicle |

Appendix B

IoT Sensor Board Interrupt Code

```
#include <WaspSensorAgr_v30.h>
#include <WaspWIFI_PRO.h>
float watermark1; //variable for storing watermark reading
uint8_t socket = SOCKET0; //socket used for wifi module
char ESSID[] = "dd-wrt"; //SSID of the AP to connect to
char PASSW[] = "hjdu6$75@"; //password of the AP to connect to
uint8_t error;
uint8_t status;
uint8_t udp_handle = 0;
uint16_t i = 0; //constant used for converting watermark frequency
char lo = 0; //constant used for converting watermark frequency
char hi = 0; //constant used for converting watermark frequency

char HOST[] = "192.168.1.105";
char REMOTE_PORT[] = "3000";
char LOCAL_PORT[] = "2000";
//Instance object
weatherStationClass weather;
watermarkClass wmSensor1(SOCKET_1);
void setup()
{
  // Turn on the USB and print a start message
  USB.ON();
  USB.println(F("Initializing"));
  // Turn on the sensor board
  USB.println(F("Entering sleep mode"));
  Agriculture.ON();
}
```

```

//RTC.OFF();
SD.setMode(SD_OFF);
ACC.setMode(ACC_POWER_DOWN);
}
void loop()
{
//Enter sleep mode
Agriculture.sleepAgr("00:00:00:00", RTC_OFFSET, RTC_ALM1_MODE4,
SENSOR_ON, SENS_AGR_PLUVIOMETER);
//check pluviometer interruption
if( intFlag & PLV_INT)
{
USB.println('\n');
USB.println(F("Wake-up"));
USB.println(RTC.getTime());
USB.println(F("Total # of wake-ups"));
USB.println(intArray[PLV_POS], DEC);
disableInterrupts(PLV_INT);
PWR.clearInterruptionPin();
intFlag &= ~(PLV_INT);

watermark1 = wmSensor1.readWatermark();

USB.print(F("Watermark1 Frequency: "));
USB.print(watermark1);
USB.println('\n');
USB.print(F("Battery Level: "));
USB.print(PWR.getBatteryLevel(),DEC);

USB.print(F(" %"));
USB.print(F(" | Battery (Volts): "));
USB.println(F(" V"));
USB.println('\n');

error = WIFI_PRO.ON(socket);
if (error == 0)
{
USB.println(F("WiFi switched ON"));
}
else

```

```

    {
        USB.println(F("WiFi did not initialize correctly"));
    }
error = WIFI_PRO.setESSID(ESSID);
    if (error == 0)
    {
        USB.println(F("WiFi set ESSID OK"));
    }
    else
    {
        USB.println(F("WiFi set ESSID ERROR"));
    }
error = WIFI_PRO.setPassword(WPA2, PASSW);
    if (error == 0)
    {
        USB.println(F("WiFi set AUTHKEY OK"));
    }
    else
    {
        USB.println(F("WiFi set AUTHKEY ERROR"));
    }
error = WIFI_PRO.softReset();
    if (error == 0)
    {
        USB.println(F("WiFi softReset OK"));
    }
    else
    {
        USB.println(F("WiFi softReset ERROR"));
    }
    if (WIFI_PRO.isConnected() == true)
    {
        USB.print(F("WiFi is connected OK"));
        USB.println('\n');
    }
error = WIFI_PRO.getIP();
    if (error == 0)
    {
        USB.print(F("IP address: "));
        USB.println(WIFI_PRO._ip);
    }

```

```

    }
    else
    {
        USB.println(F("getIP error"));
    }
error = WIFI_PRO.getGateway();
if (error == 0)
{
    USB.print(F("GW address: "));
    USB.println(WIFI_PRO._gw);
}
else
{
    USB.println(F("getGateway error"));
}
error = WIFI_PRO.getNetmask();
if (error == 0)
{
    USB.print(F("Netmask address: "));
    USB.println(WIFI_PRO._netmask);
}
else
{
    USB.println(F("getNetmask error"));
}
error = WIFI_PRO.setUDP(HOST, REMOTE_PORT, LOCAL_PORT);
// check response
if (error == 0)
{
    // get UDP handle
    udp_handle = WIFI_PRO._socket_handle;
    USB.print(F("Open UDP socket OK in handle: "));
    USB.println(udp_handle, DEC);
}
i = (uint16_t) watermark1;
char lo = i & 0xFF;
char hi = i >> 8;
uint8_t data[] = {hi, lo};
error = WIFI_PRO.send( WIFI_PRO._socket_handle, data, 2);
// check response

```

```

    if (error == 0)
    {
        USB.println(F("Send data OK"));
    }
    else
    {
        USB.println(F("Error calling 'send' function"));
        WIFI_PRO.printErrorCode();
    }
    WIFI_PRO.OFF(socket);
    USB.println(F("WiFi switched OFF"));
    USB.println(F("Entering sleep mode"));
    USB.println(RTC.getTime());
}
}

```

Sample Output

Initializing

Wake-up

Total # of wake-ups

1

Watermark1 Frequency: 8333.3330078125

Battery Level: 73 % | Battery (Volts): 3.9990000724 Volts

WiFi switched ON

WiFi set ESSID OK

WiFi set AUTHKEY OK

WiFi softReset OK

WiFi is connected OK

IP address: 192.168.1.124

GW address: 192.168.1.1

Network address: 255.255.255.0

Open UDP socket OK in handle: 0

Send Data OK

WiFi switched OFF

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