AMERICAN UNIVERSITY OF BEIRUT

# DESIGN OF A NEW MINIATURIZED MICROWAVE VECTOR NETWORK ANALYZER

by
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# ABSTRACT
# OF THE THESIS OF

Renee Youssef Abi Khalil for Master of Engineering
Major: Electrical and Computer Engineering

Title: Design of a New Miniaturized Microwave Vector Network Analyzer

A Vector Network Analyzer (VNA) is a microwave measurement device that is used to characterize different Radio Frequency (RF) components. It measures the scattering parameters of RF devices in order to determine their electrical behavior for an accurate characterization and analysis of RF circuits.

The VNA consists of many RF components that are connected together in order to enable suitable S-parameters measurement of a device under test (DUT). In addition, a software controls the interaction between the different components and the DUT in order to determine its parameters and characteristics.

The focus of this thesis is on the novel design of one component in the RF chain of the VNA. This component, which is the power divider, is responsible for dividing the input RF power into two output branches. This thesis presents a new continuous phase-tunable Wilkinson power divider. The tuning of the power divider enables the extraction of a variable phase difference between the two output ports of the power divider. The presented power divider is compact, reconfigurable and relies on two varactor diodes to achieve output phase tuning between $0^o$ and $55^o$.

The proposed design maintains very good impedance matching and isolation across the entire operating bandwidth from 2 GHz to 3.8 GHz and across all the various phase states. Such tuning potential of the power divider enables its wide integration into advanced VNA RF chains, feeding networks of phased arrays, and new communication platforms.

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# ABBREVIATIONS

VNA: Vector Network Analyzer

RF: Radio Frequency

DUT: Device under Test

BPF: Band Pass Filter

EM: Electro Magnetic

S-Parameters: Scattering parameters

ISM band: Industrial, Scientific, and Medical radio band

TL: Transmission Line

LO: Local Oscillator

IF: Intermediate frequency

LNA: Low Noise Amplifier

PD: Power Divider

DC: Directional Coupler

ADS: Advanced Design System

DA: Data Acquisition

LPF: Low Pass Filter

# CHAPTER 1

# INTRODUCTION

A vector network analyzer (VNA) is a multi-port device used to characterize different Radio Frequency (RF) components. It measures the scattering parameters of RF devices in order to determine their electrical behavior for an accurate characterization and analysis of RF circuits. It mainly computes and illustrates the amount of reflection and transmission through the DUT's ports.

S-parameters are a description of the response of an N-port network to signal(s) incident to any or all of the ports. The first number in the subscript of an S-parameter refers to the responding port, while the second number refers to the incident port. Thus, $S_{31}$ means the response at port 3 due to a signal at port 1.

S-parameters measurements compute the amount of reflection and transmission among different ports of a device. One-port VNAs are designed to measure the reflection coefficient $S_{11}$ of a one-port RF device such as an antenna. Two-port VNAs are designed to measure the four S-parameters ($S_{11}$, $S_{12}$, $S_{21}$, and $S_{22}$) of a two-port device such as filters, attenuators, amplifiers or other two-port components.

The internal system of a VNA is composed of a chain of RF circuits that are connected together as shown in Figure 3. Such an RF chain is composed of mixers, couplers, power dividers, amplifiers, and attenuators that are arranged in order to enable the whole system to evaluate the various reflection and transmission coefficients of a device.

The functionality of a VNA can be summarized as illustrated in Figures 1 and 2 [1]. When an incident wave (Wave R) hits the input port of a device, part of it will be

transmitted (Wave B) and the rest will reflected back (Wave A). The magnitude and the phase of these three waves should be evaluated in order to calculate the S-parameters of a DUT [2].

Each block of a VNA is by itself defined by its S-parameters, impedance bandwidth and operational frequency range. Such blocks are built by taking into consideration their theoretical analysis and appropriate impedance matching techniques [3] in order to reduce the amount of losses and ensure an optimal transfer of power among them.

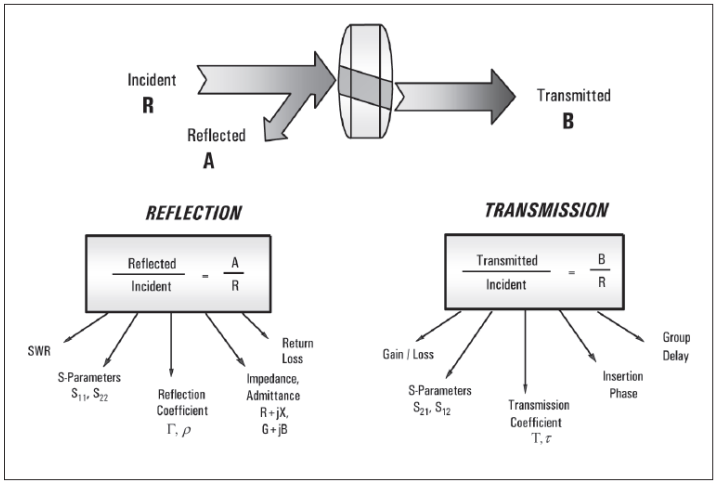



Figure 1 The VNA functionality [2]

In this report, the details of designing a VNA, along with the functionalities of the different incorporating blocks, are discussed. This thesis focuses on proposing and designing one VNA block, the power divider, with phase tuning capabilities. Such phase-tunable power divider, which is the main contribution of this thesis, relies on

embedding some active components within its structure to tune the phase difference between its output ports.

Chapter two of this thesis report provides a theoretical view of the VNA aspects. Chapter three provides a literature review that presents the most recent research work on VNAs. Chapter four discusses the different RF components used to build a VNA along with the design of a novel phase tunable power divider. Chapter five discusses the error detection techniques. Chapter six introduces the software part, which relates to the computation of the actual S-parameters. Chapter seven concludes this thesis and discusses some future work aspects.

# CHAPTER 2

# BACKGROUND REVIEW OF THE VNA ASPECTS AND THE S-PARAMETERS

In order to design a VNA, there are many concepts that need to be addressed. This chapter includes some main sections that illustrate such important concepts and the relation between the VNA and the S-parameters.

## 2.1. RF devices as 2-port networks

A 2-port RF device is illustrated in Figure 2. The wave associated with each port has incident and reflected components.

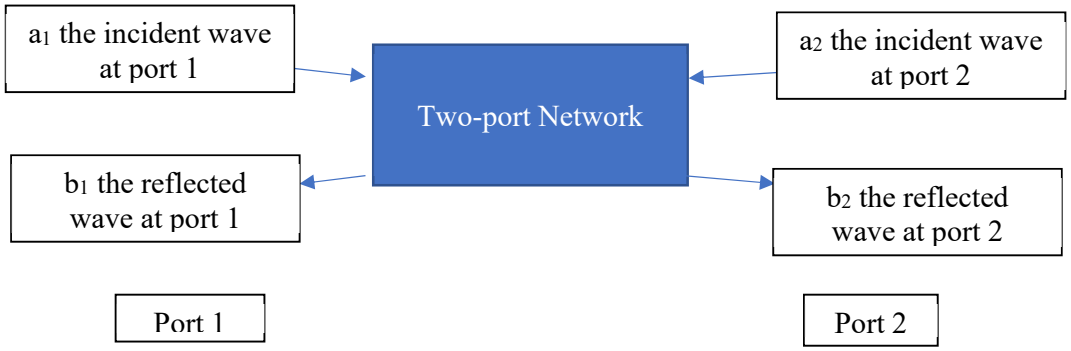



Figure 2 A two port network input and output description

The voltages and currents are no longer used to characterize the network. However, it is characterized by the forward and backward waves that form a standing wave perspective as highlighted in transmission line theory [3].

For an n-port network, power wave components are associated with:

$a_n = \frac{V_{0n}^+}{\sqrt{Z_{0n}}}$ and $b_n = \frac{V_{0n}^-}{\sqrt{Z_{0n}}}$ (1)

Where $V_{0n}^- \; and \; V_{0n}^+$ are the voltages of the forward and backward waves at port n.

### 2.2. The S-parameters analysis

For 2-port networks, the S-parameters matrix is defined as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (2)$$

Where in general: $S_{i,j} = \frac{b_j}{a_i}\Big| \; a_k=0$ with k≠i. So in particular:

- $S_{11}$ represents the reflection coefficient at port 1 and is equal to:

$$\frac{reflected\ signal\ at\ port\ 1}{incident\ signal\ at\ port\ 1} = \frac{b1}{a1}\Big|_{a2=0} \quad (3)$$

- $S_{21}$ is the transmission coefficient at port 2 and is equal to:

$$\frac{transmitted\ signal\ at\ port\ 2}{incident\ signal\ at\ port\ 1} = \frac{b2}{a1}\Big|_{a2=0} \quad (4)$$

- $S_{12}$ is the reverse transmission coefficient at port 1 and is equal to:

$$\frac{reverse\ transmitted\ signal\ at\ port\ 1}{reverse\ incident\ signal\ at\ port\ 2} = \frac{b1}{a2}\Big|_{a1=0} \quad (5)$$

$S_{22}$ is the reverse reflection coefficient at port 2 and it is equal to:

$$\frac{reverse\ reflected\ signal\ at\ port\ 2}{reverse\ incident\ signal\ at\ port\ 2} = \frac{b2}{a2}\Big|_{a1=0} \quad (6)$$

In order to set $a_k=0$, port k should be terminated with a matched load. Such S-parameters are measured using the ratio of the power waves entering and leaving port j, while inputting a wave at port i [4].

### 2.3. Theoretical View of the Network analyzer along with VNA types

Measuring and identifying the S-parameters of a microwave device is essential in the characterization of such a device and understanding its operation, implementation

and circuit integration. S-parameters characterize the performance of a microwave device in regards to incident, transmitted and reflected signals.

### *2.3.1. Scalar and Vector Network analyzer*

First, network analyzers can be built in a scalar way, i.e. to measure only the magnitudes of the signals. However later on, network analyzers have been upgraded to be Vector Network analyzers so that they can measure both magnitudes and phases of signals [5]. Because reflection and transmission coefficients are complex numbers, identifying the magnitude and the phase of various S-parameters is instrumental.

### *2.3.2. "1-port" VNA*

A 1-port VNA is used to measure the $S_{11}$ of a 1-port RF device such as an antenna. The VNA mainly sends an incident signal to the antenna and calculates the reflected power at its port. It can do so because it mainly consists of an RF source, LO (Local Oscillator) source, Power divider, directional coupler, mixer, amplifiers and filters. Each one of these components is detailed in chapter 4. The corresponding block and circuit diagrams are shown in Figure 3.

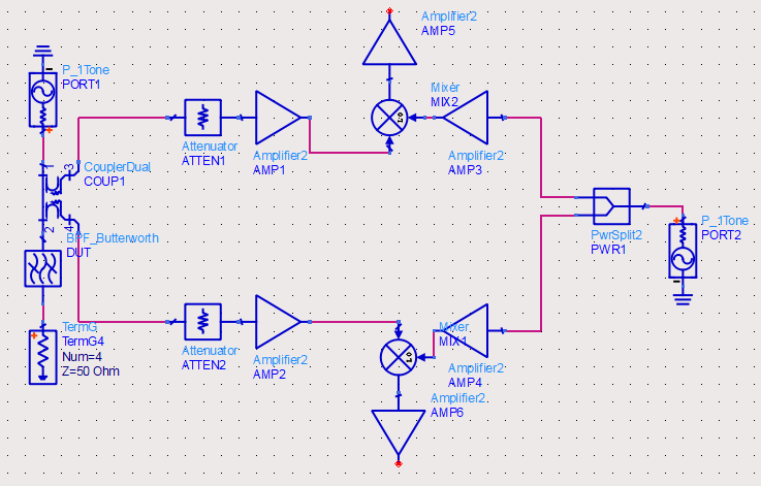



Figure 3 1-port VNA circuit diagram

The RF input source generates a sinusoidal signal with a given amplitude power and at a certain frequency. Then, the coupler couples this signal by dividing the circuit to two symmetrical paths. One to get the reflected power and the other one to extract the incident power to compute their ratio and get $S_{11}$.

The coupled power, which is decreased by the coupling factor of the coupler, will be amplified back by an amplifier until it reaches the RF input port of the mixer. However, a Local Oscillator generates a signal at a given frequency and a power divider divides this signal power to two equivalent powers that go each to a path. This divided power signal will be amplified until it arrives to the LO input of the mixer. The mixer mixes these two inputs and outputs an IF (Intermediate Frequency) signal, which will also be amplified in order to get this power (magnitude and phase).

The same scenario happens on the reflected path, but the only difference here is that the RF input signal hits the device under test (DUT), and the reflected signal is coupled by the coupler through its isolation port. The reason behind this is explained in the Directional Couplers' section of chapter 4. This reflected signal will be amplified

and the same scenario, of the incident path, will be repeated. After the two mixers mix the inputs and provide the two IF output signals, a1 and b1, a signal processing device will save these 2 parameters in order to calculate the $S_{11}$.

Noting that, a frequency sweeping process will be applied to make the VNA a broadband one. When sweeping the frequency, the first stage of getting the a1 and b1 points is to do a calibration stage in order to detect and correct the errors, which were described by [6] and discussed in chapter 5.

### *2.3.3. "2-port" VNA*

A VNA can also be a multi-port system. In fact, an n-port VNA can extract $2^n$ S-parameters, hence a 2 port-device extracts 4 S-parameters; $S_{11}$, $S_{21}$, $S_{12}$, $S_{22}$. The first index represents the testing port and the second represents the port of the incident signal. $S_{21}$, for example, means that port 2 is being tested when the incident signal is at port 1.

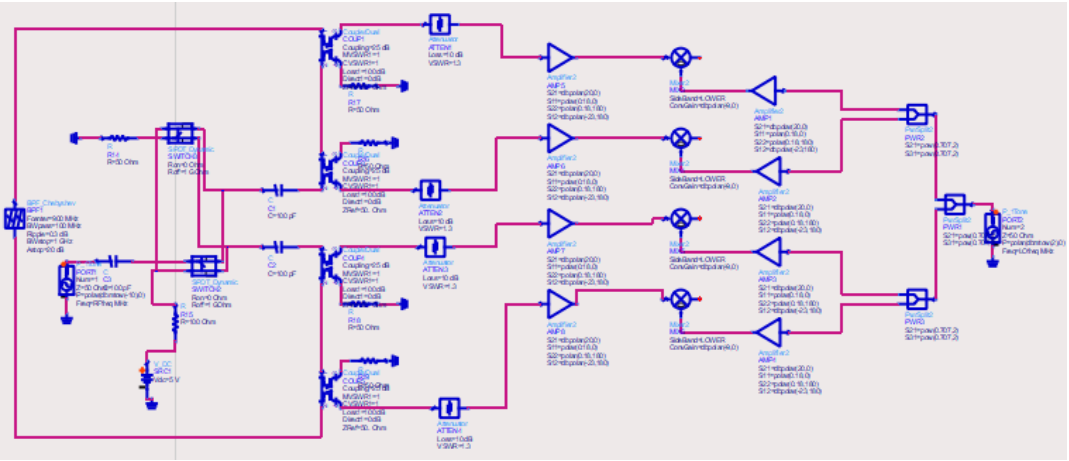


Figure 4 2 port VNA

For the 2-port VNA, two external sources are needed. The first source is the RF, which is used as the incident signal on the circuit. The other one is the Local Oscillator (LO), which is used by a mixer to either down-convert or up-convert the frequency of the outputs. This VNA has 2 switches to route the RF signal to the couplers, using either port 1 or port 2. When the signals reach the couplers, the same scenario as the 1 port VNA occurs. The main difference is that instead of having 2 paths, like the 1-port VNA, a 2-port VNA has 4 paths and it has 4 outputs, which are $a_1$, $b_1$, $a_2$, $b_2$. It is important to note that 2-port VNAs need also to be calibrated as will be discussed in chapter 5.

# CHAPTER 3

# LITERATURE REVIEW

Many researchers have explored various VNA designs, architectures and techniques. In this chapter, we explore the various work executed in the literature on various VNA types.

In [3], a planar 2-port VNA is designed with few components needed. The RF components used to build this VNA are couplers, attenuators, power dividers, amplifiers and mixers. The couplers were built and realized on a printed circuit board (PCB) due to their ease of fabrication. Figure 5 shows the fabricated prototype of the VNA. However, Figure 5 shows a comparison between the S-parameters of a 6-dB attenuator measured using a compact VNA and the designed VNA.

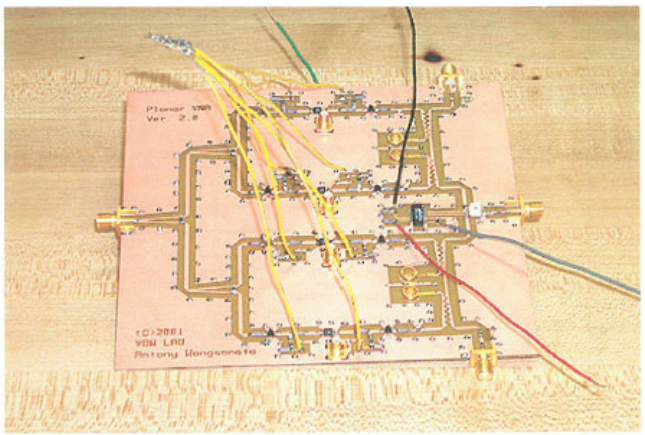


Figure 5 Proposed VNA [3]

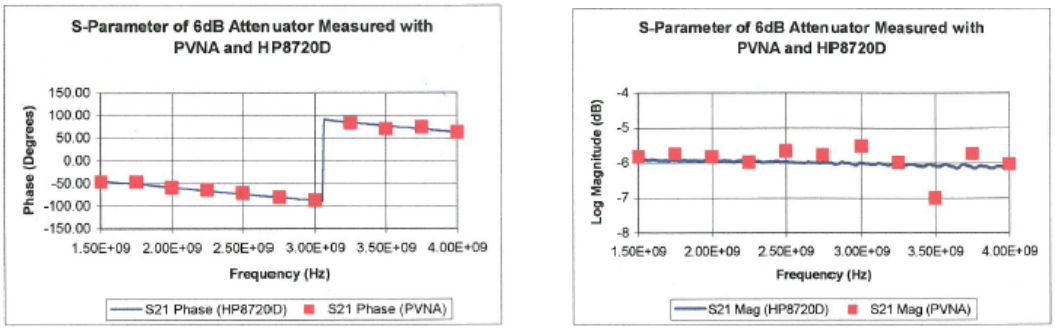



Figure 6 Results (Mag and Phase) [3]

In [5], a 1-port VNA is designed for high school usage. Integrated Ciruits (IC) chips were bought off the shelf in order to build such a VNA. Figure 7 represents the PCB schematic of the VNA and Figure 8 shows the comparison results of the proposed VNA with the Agilent VNA N5232A PNA-L Microwave Network Analyzer [6]. A coupler, power divider, some amplifiers and mixer chips were used in this work.

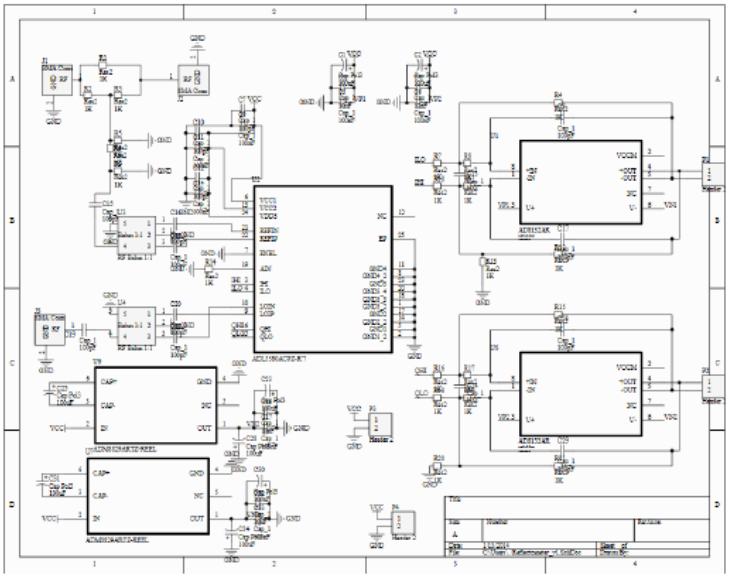


Figure 7 PCB Schematic [5]

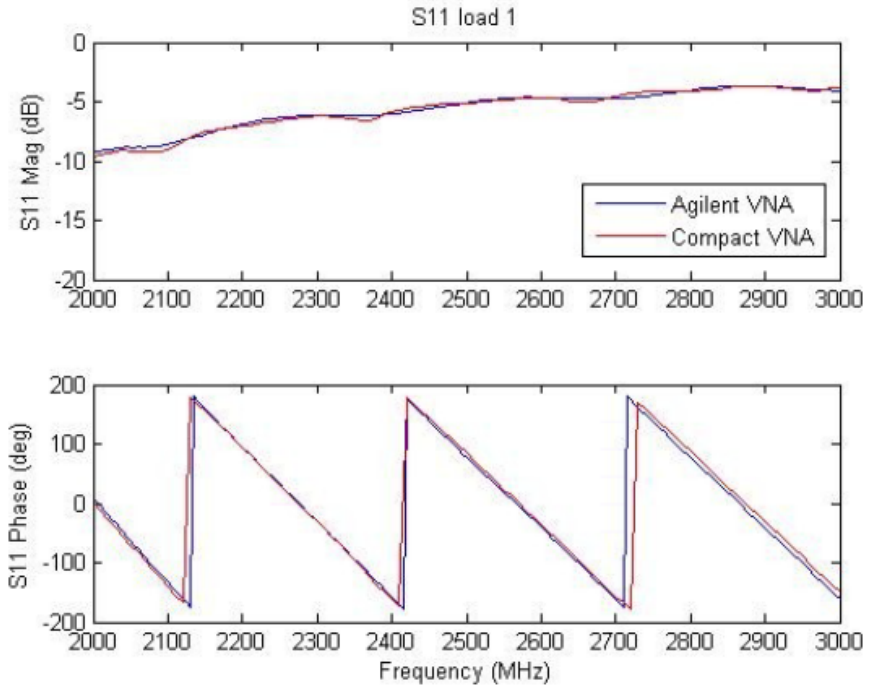



Figure 8 Results of comparison [5]

In [7], a tri-band 2-port VNA is presented for biomedical concentration measurements. It consists of a six-port-junctions network and it is designed to function with a 10% bandwidth around 6.6 GHz, 19.7 GHz and 32.4 GHz. Such parameters can be calculated using appropriate calibration techniques [7]. The design, shown in Figures 9 and 10, employs a coupler connected to the DUT from one side and to an attenuator on the other side. This attenuator is connected to a power divider and two 6-port RF-Power detectors. The circuit chain is then connected to an ADC, which is driven by a Matlab code.

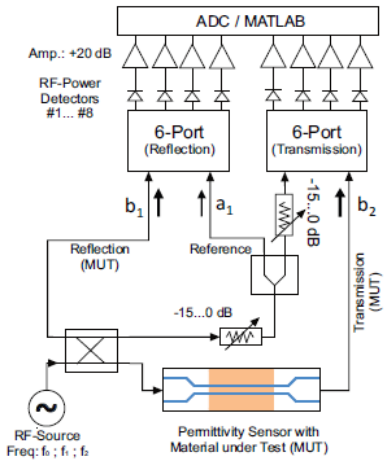



Figure 10 Schematic the Reflectometer [7]

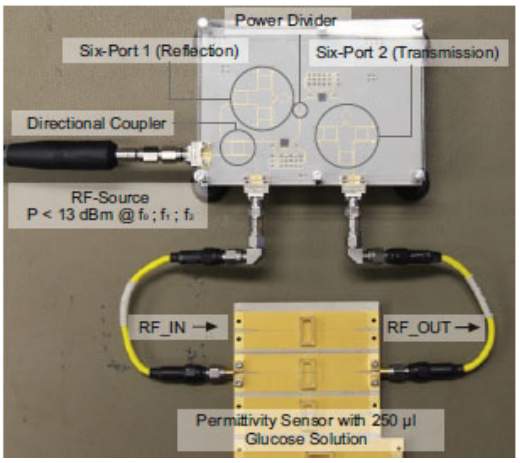



Figure 9 Fabricated prototype [7]

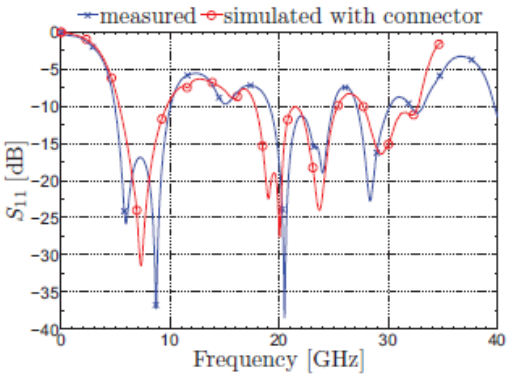



Figure 11 Results of the simulation vs. measurements [7]

# CHAPTER 4

# RF SYSTEM OF A VNA

## 4.1. Introduction to the VNA Architecture

Various RF components constitute the VNA. It is built by combining a chain of RF component. First of all, an RF signal (1) is incident into the input port of the VNA from side 1, and a Local Oscillator signal 2 is incident on port 2 of the VNA. Signal 1 enters into the input port of a directional coupler and signal 2 enters into the input port of a power divider. The coupler will couple the signal into its ports, which will result in having 2 signals divided into 2 paths. On the other hand, the divider will divide the signal into 2 equal signals through the 2 paths. The through port of the coupler should be connected to DUT.

After the 2 ports of the coupler, an attenuator should be placed in order to attenuate the signals coming from the other side of the VNA (the local oscillator signal side) where clearly, the signal coming out of the coupler will be attenuated too. Thus, an amplifier should be placed after the attenuator to amplify back the signal. Knowing that the attenuator is reciprocal and the amplifier is not, the amplifier will only amplify the signals coming out of the attenuator.

On the other side (the local oscillator signal side), an amplifier is placed after the power divider to amplify back the signal that was divided by half by the power divider. The first amplifier will be connected to the RF input port of a mixer, and the output signal of the second amplifier will be connected to the LO port of the same mixer. Then this mixer will mix the two signals, resulting in an intermediate frequency (IF) signal

which will be collected and saved in order to be used in the calculation of the S-parameters. This same chain of connected components should be the same along the 2 paths that were created due to the coupler and the power divider.

## 4.2 Power Dividers

A power divider is a passive RF component that is used to typically divide the power coming from one input into several outputs. The simplest type is a simple T-junction. It is a 3-port device that divides the input power into two output powers [4].

### *4.2.1. Introduction to the Wilkinson power divider*

Another popular power divider that can be matched and isolated at all ports is the Wilkinson power divider that is shown in Fig. 12 [4], with its internal circuitary shown in Fig. 13 [4].

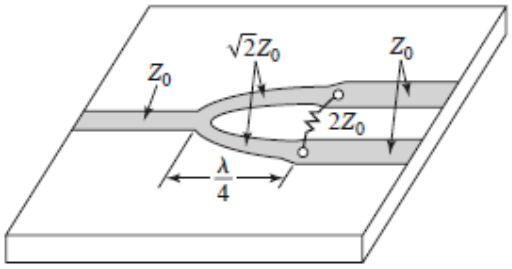



Figure 12 . The Wilkinson power divider in microstrip form [4]

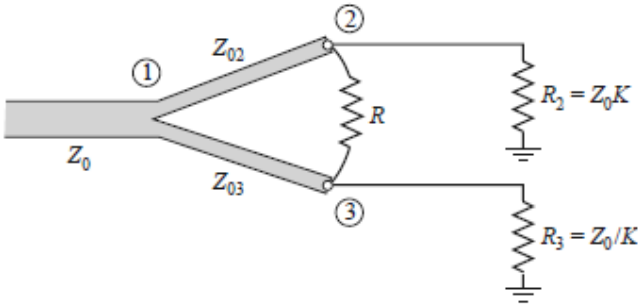



Figure 13 The Wilkinson power divider circuit [4]

There are multiple power distributions that can be used in a Wilkinson power divider; however, the 3-dB Wilkinson power divider is the most common one. In fact, a 3-dB Wilkinson power divider splits the incident power, at port 1, into two equal powers that are, each, equal to the one-half of the incident power.

By analyzing the topology in figure 12, the following equations are concluded:

$K^2 = \frac{P_3}{P_2}$ (K is the power ration between the output ports) (7)

$Z_{03} = Z_0 \sqrt{\frac{1+K^2}{K^3}}$ (8)

$Z_{02} = K^2 * Z_{03} = Z_0 * \sqrt{K(1+K^2)} = Z_0 * Z$ (9)

$R = Z_0 * (K + \frac{1}{K})$ (10)

Adding that $Z_{in} = \frac{Z^2}{2}$ with $Z = \sqrt{K(1+K^2)}$ (11)

Where $Z_{in}$ is the impedance looking from the input port to the output ports.

And for the equal split case, $P_2 = P_3$ ➔ K=1 (12)

⇨ $R = Z_0 * (1 + \frac{1}{1}) = Z_0 * 2$ (13)

⇨ $Z_{02} = 1^2 * Z_{03} = Z_0 * \sqrt{1(1+1^2)} = Z_0 * \sqrt{2}$ (14)

⇨ $Z_{03} = Z_0 \sqrt{\frac{1+1^2}{1^3}} = Z_0 * \sqrt{2}$ (15)

⇨ $Z = \sqrt{1(1+1^2)} = \sqrt{2}$ (16)

⇨ $Z_{in} = \frac{(\sqrt{2})^2}{2} = 1$ (17)

When all ports are terminated with matched loads, the reflection at port 1 is found to be equal to 0 ➔ $P_1^- = |S_{11}|^2 * P_1^+ = 0$ (18)

And $P_2^- = P_3^- = \frac{P_1^+}{2}$ (19)

So in summary, the following are obtained:

⇨ $S_{11} = 0$ ( $Z_{in} = 1$ at port 1) (20)

⇨ $S_{22} = S_{33} = 0$ (ports 2 and 3 are matched) (21)

⇨ $S_{12} = S_{21} = S_{13} = S_{31} = -\frac{j}{\sqrt{2}}$ (symmetry between ports 2 and 3) (22)

⇨ $S_{23} = S_{32} = 0$ (short or open at bisection) (23)

So in summary, the S-parameters matrix will be as the following: [4]

$$S = \begin{bmatrix} 0 & -j/\sqrt{2} & -j/\sqrt{2} \\ -j/\sqrt{2} & 0 & -j/\sqrt{2} \\ -j/\sqrt{2} & -j/\sqrt{2} & 0 \end{bmatrix} \quad (24)$$

A schematic, built on ADS [11], is shown below in Figure 14 and its corresponding simulated results are shown in Figure 15, in order to show the functionality of this Wilkinson power divider as follows:

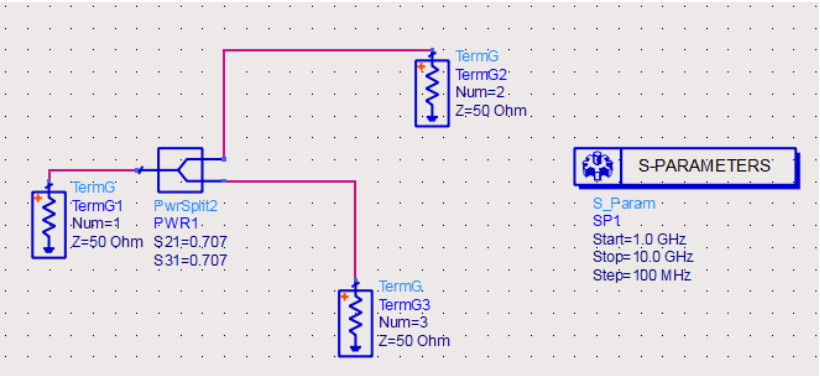



Figure 14 ADS schematic of a built-in Power Divider block

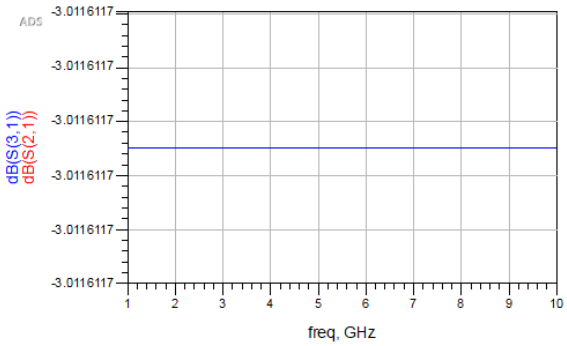



Figure 15 ADS results of the PD

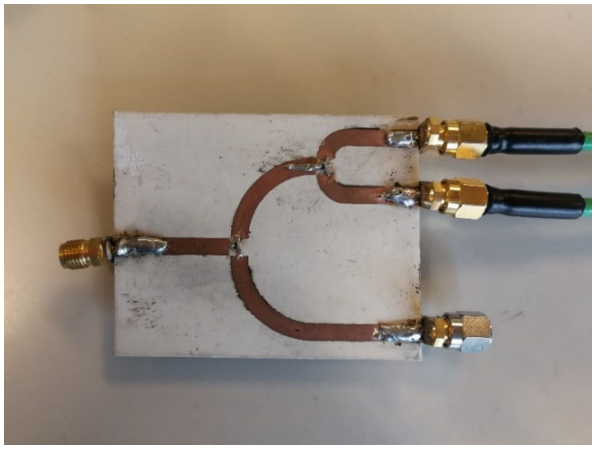


Figure 16 Fabricated power divider

In Figure 16, a 6 dB power divider is designed and fabricated in order to understand its topology and understand its functionality. In addition, a two-stage 3 dB power divider is designed and analyzed. A two stage power divider is built using two power dividers connected to each other. If 2 3-dB power dividers are used, the output port of the first one should be connected to the input port of the second and the signal will be divided twice. This results in having the incident signal power decreased by 6 dB, or divided by 4. So if the 2 output ports of the first power divider are connected to 1 power divider each, 4 paths will be created. In Figure 16, 2 paths were only needed, so the second output port of the first power divider was terminated by a 50 Ohms load.

### *4.2.2. Previous work on power dividers*

After having a look at previous works done on power dividers, it was noticed that many researches were working on designing either an in-phase power divider or an out-of-phase power divider. Figure 17 shows a power divider, previously designed, that only has an out-of-phase component. Its S-parameters are shown In Figure 18, where it is clear that it has a 180 degrees phase difference between its 2 output ports.

Figure 17 Fabricated prototype [35]

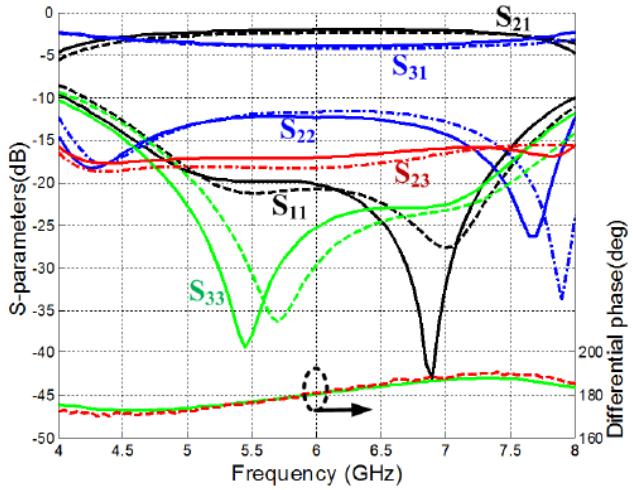



Figure 18 S-parameters of the fabricated prototype [35]

Other works reported a power divider with in-phase and out-of-phase components, as shown in Figure 19. Figures 20 and 21 show the measured S-parameters of the fabricated design, while comparing them to the simulated ones for both in-phase and out-of-phase cases. In [36], a phase shifter was connected to the power divider in order to switch the phase between 0 and 180 degrees.

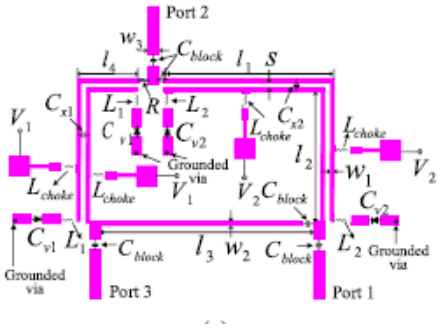



Figure 19 Circuit of the designed power divider [36]

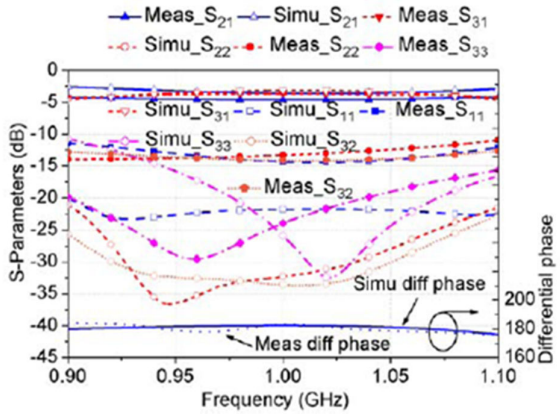



Figure 20 S-parameters (measured vs simulated) of the out-of-phase state

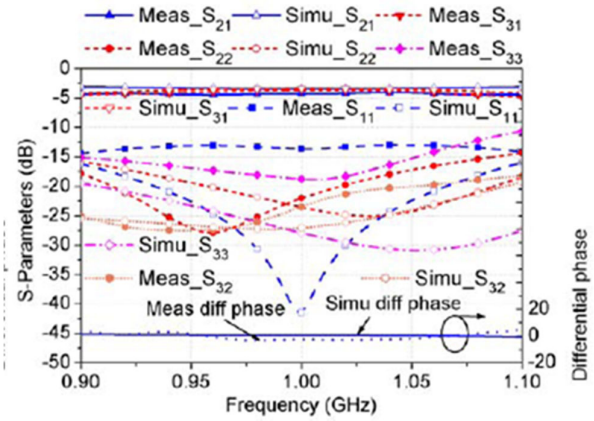



Figure 21 .S-parameters (measured vs simulated) of the in-phase state

### *4.2.3. Design of a novel Wilkinson power divider*

However, no work related to designing an in-phase and tunable out-of-phase power divider was reported in the literature. In this thesis, a tunable phase power divider was designed, fabricated and measured. This power divider has an in-phase and tunable out-of-phase characteristics.

Figure 22 shows the layout of a designed microstrip power divider, on ADS[11]:

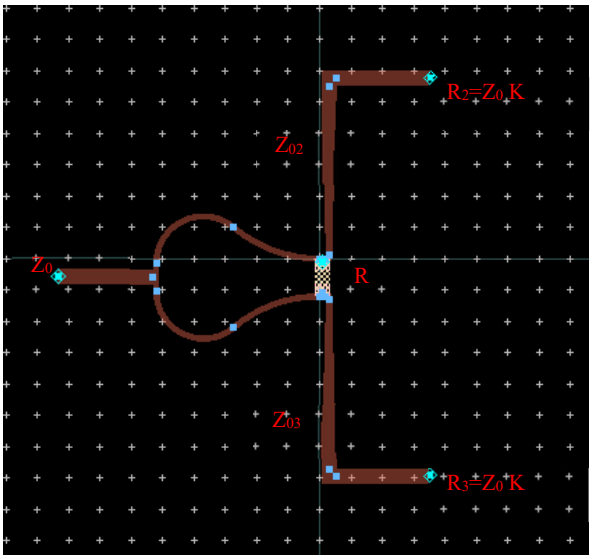



Figure 22 Layout of a power divider

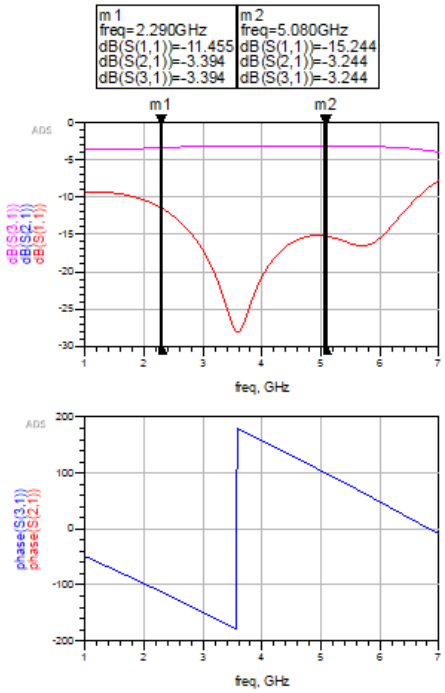



Figure 23 Results of the designed power divider

Figure 22 shows the layout of a 3 dB power divider designed on a RO3010 board, taking into consideration all the required values. Figure 23 shows the simulated

S-parameters of this designed Wilkinson power divider prior to adding the tuning structure. It is a simple power divider structure with a broadband frequency range of operation. $S_{11}$ is matched along the bandwidth starting from 2 GHz to 6.5 GHz, having the $S_{21}$ and $S_{31}$ around -3 dB (Since a 3 dB power divider was intended to be designed) along the whole operational bandwidth.

Moreover, after investigating previous work in the literature on power dividers, an important point was noticed. Extensive studies are done on improving in-phase and out-of-phase power dividers as two different components. Also, some researchers worked on combining the in-phase and constant out-of-phase behaviors in one power divider. However, no work has been done on proposing a single power divider that has an in-phase and tunable out-of-phase behavior.

Thus, in this thesis, a novel tunable-phase Wilkinson power divider is proposed and designed. This device will have an in-phase and a tunable out-of-phase behavior. Adding a tuning ability that can enable a continuous tunable phase difference between the output ports of the power divider necessitates loading one of the ports with a varactor diode.

Hence, once the varactor is actively biased, any change in the supplied voltage results in a capacitance change of the diode. This change of capacitance leads to a change of the effective electric length of the transmission lines composing the new topology of the power divider. Such a change in the electrical length leads to tuning of the phase difference between the output ports. Changing the electrical length of the transmission lines leads to a mismatch and a change in the magnitude of the reflection coefficient at the input port. Overcoming such mismatch can be achieved by introducing

a multi-stage power divider that is connected to the initial Wilkinson power divider of Figure 21.

Furthermore and in order to avoid an extra 3 dB loss at the output, a 3 dB power combiner is integrated into the multi-stage divider. A cascade of a divider-combiner topology, after the location of the varactor, results in overcoming the anticipated losses and maintaining the magnitude of the signal while adding a significant tuning ability.

The size of this tunable multi-stage power divider is kept compact by meandering the divider-combiner structures and hence resulting in a topology that mimics the infinity symbol as shown in Figure 24. This meandered infinity shaped loop is also used to decrease the mismatch at the design's ports. Biasing networks were built to supply a voltage to the varactors. The same structures, added to port 2, should be added to port3 to avoid having high insertion losses.

A second varactor is added to the topology, as shown in Figure 24, in order to enhance the phase variation ability of the design. The in-phase component is maintained by adding a similar section to port 3 of the Wilkinson power divider of Figure 22.

Figure 24 represents the layout of the new proposed design.

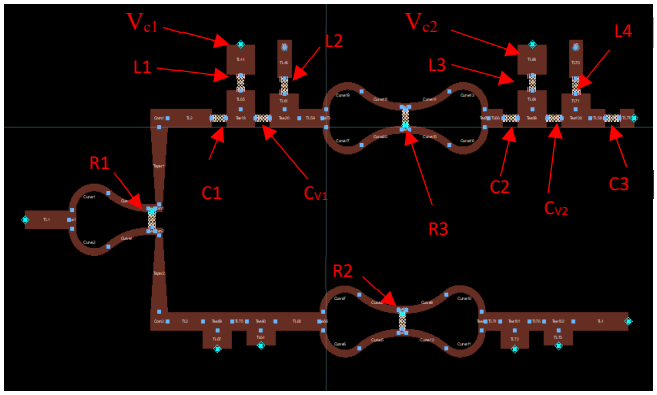



Figure 24 Layout of the proposed design

In order to activate the varactor diodes, biasing networks are built and integrated into the design. These biasing lines are of high impedance, with RF chokes being integrated, to ensure appropriate biasing.

These biasing networks are composed of RF chokes to avoid RF signals leakage into the power supplies and of DC blocks to prevent the DC signals from mixing with the RF signals and supplies. The values of these elements are shown in Table 1. The reflection coefficient of the tunable power divider for variable voltage supply is shown in Figures 25 and 27. Figure 25 represents the reflection coefficients when $V_{C1}=V_{C2}= 0V$ and Figure 27 shows the reflection coefficients of $V_{C1}=V_{C2}= 4V$.

Various voltage states are supplied to the varactors, leading to different phase differences between the two output ports (phase ($S_{21}$-$S_{31}$)). Three voltages supplies are shown in this thesis report, and the S-parameters were investigated to guarantee the effectiveness of the design proposed.

When supplying 0V, to each varactor, the simulated reflection coefficients ($S_{11}$, $S_{22}$, $S_{33}$) are found as shown in Figure 25.The transmission coefficients ($S_{21}$, $S_{31}$), along with the isolation coefficient($S_{23}$), are shown in Figure 26.

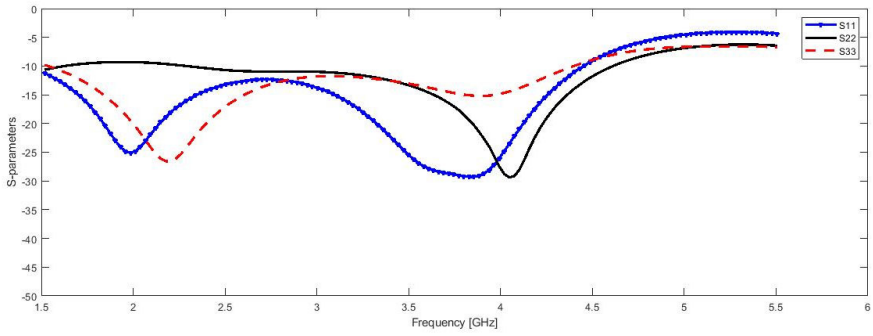



Figure 25 Reflection coefficients at $VC_1=VC_2=0V$

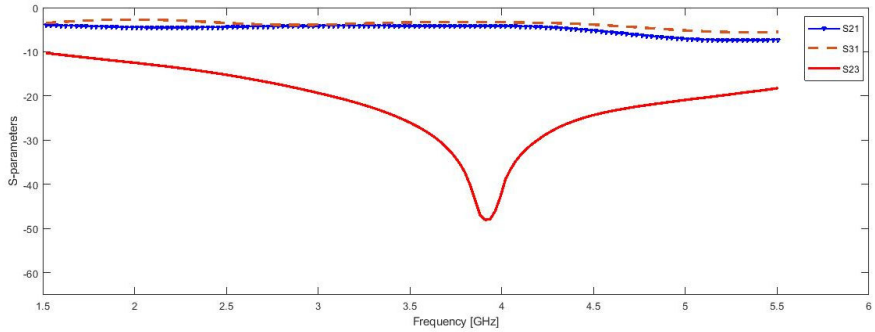



Figure 26 Transmission coefficients and isolation when $VC_1=VC_2=0V$

Knowing that the maximum supplied voltage the varactor is 8V, a middle value was chosen (i.e. 4V supply to the varactors). Upon supplying 4V to each varactor, the simulated S-parameters results are found as shown in Figure 27.

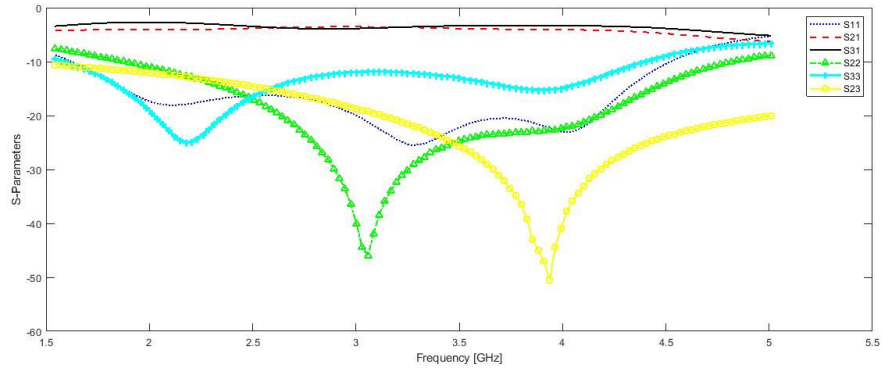



Figure 27 Simulated results of the proposed design at $VC_1=VC_2=4V$

In order to test the full capacity of this design, the maximum voltages are applied. Hence, figures 28 and 29 show the S-parameters when an 8V dc voltage is supplied to the two varactors.

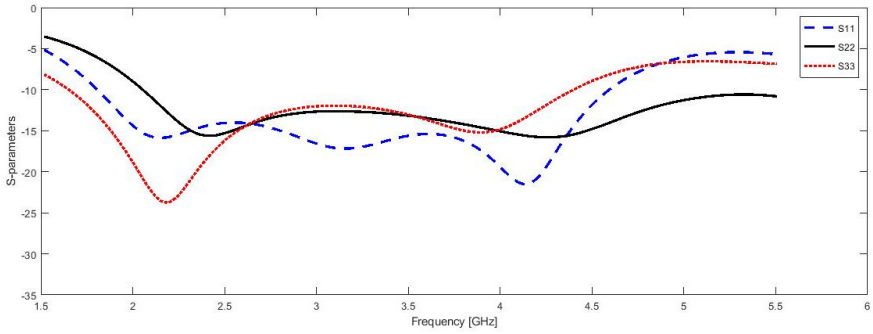



Figure 28 Reflection coefficients at VC1=VC2=8V

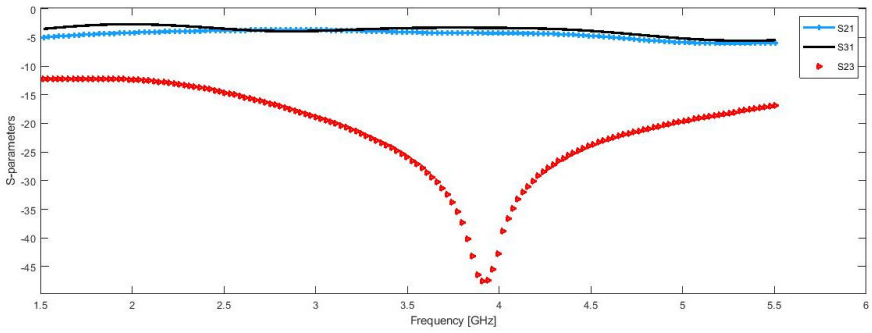



Figure 29 S21, S31 and S23 at VC1=VC2=8V

However, many other states were also investigated but the ones mentioned so far are discussed in this work.

### *4.2.4. Fabrication of the new design*

The proposed design was fabricated on a Rogers RO3010 substrate with a relative permittivity εr=10.2 and thickness H=1.27 mm. The LineCalc tool, in Advanced Design system (ADS), was used to compute the widths of 50 Ω and 70.7 Ω lines and they were found to be $w_1$= 1.2 mm and $w_2$= 0.5 mm, respectively. The varactors used, in the design, are SMV1249-079LF [38]. Figure 30 shows the fabricated prototype of the proposed design.

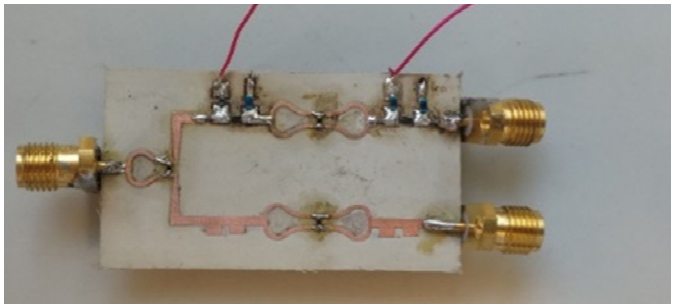


Figure 30. Fabricated design

Table 1 Values of the lumped elements used

| $R_1$ | $R_2$ | $R_3$ | $C_1$ | $C_2$ |
|---|---|---|---|---|
| 100 Ω | 50 Ω | 50 Ω | 470 pF | 470 pF |
| $C_3$ | $L_1$ | $L_2$ | $L_3$ | $L_4$ |
| 470 pF | 39 nH | 39 nH | 39 nH | 39 nH |

Table 1 shows the values used to implement the proposed design. $C_1$, $C_2$, $C_3$ are the DC blocks and $L_1$, $L_2$, $L_3$, $L_4$ are the RF chokes (RFCs). At t=0, when 0 V is applied on both $V_{C1}$ and $V_{C2}$, no phase difference will be shown between the two outputs (i.e. In-phase component). However, when varying the voltages supplied, a variable phase difference will result (i.e. a variable out-of-phase component). As a result, this design simultaneously offers an in-phase and variable out-of-phase characteristics. Figure 31 shows the measured results of the proposed fabricated design when $V_{C1}$=$V_{C2}$=4V.

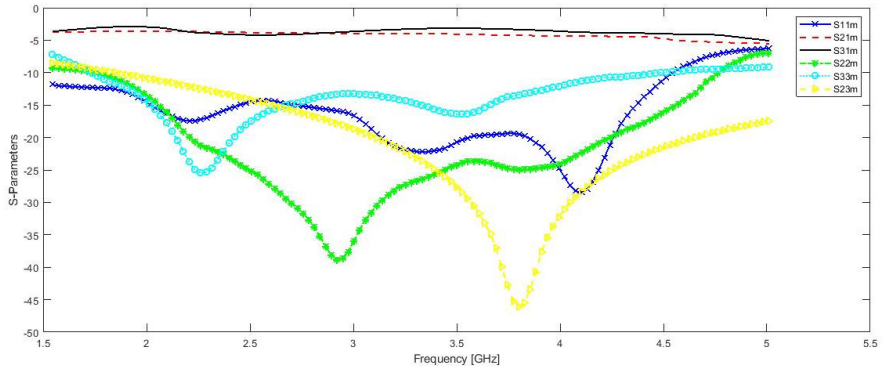



Figure 31 Measured results for VC1=VC2=4V

For this state, the corresponding reflection coefficients at each port, are less than -10 dB at the edges of the operational bandwidth of interest (2 - 3.85 GHz). Add on this, $S_{21}$ and $S_{31}$ are equal to -3.1±0.5 dB in the simulated and measured results. Figures 32 and 33 show a superposition of the reflection and the transmission coefficients, respectively, of the simulated and measured results when VC1=VC2=0V.

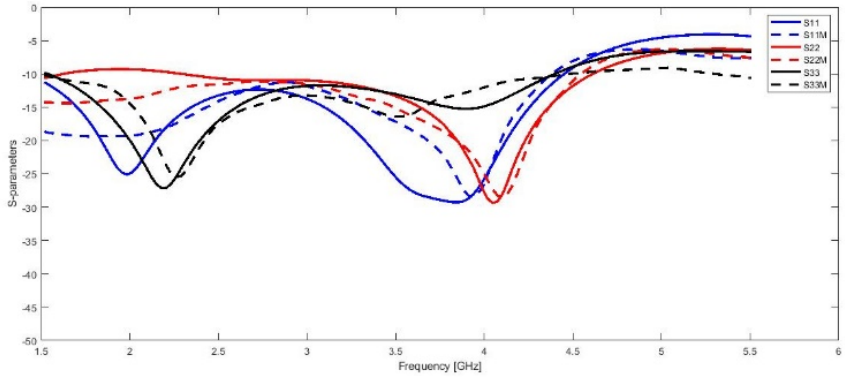



Figure 32 Reflection coefficients (Sim vs Meas) when VC1=VC2=0V

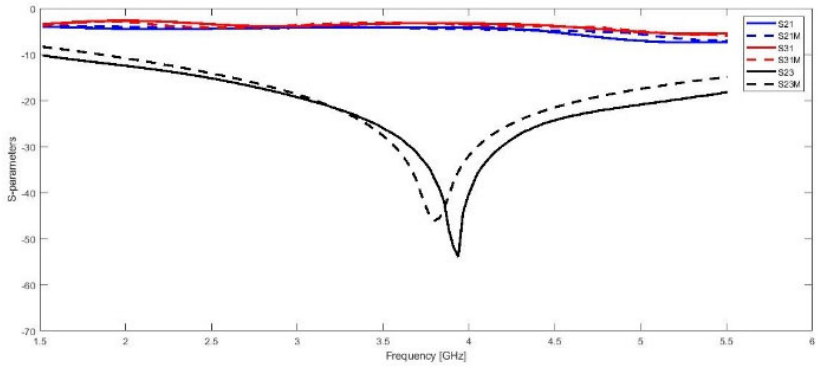



Figure 33 S21, S31 and S23 (Sim vs measured) when VC1=VC2=0V

The results show a good agreement between the simulated results and the measured one. Two additional states are also plotted. When having a 50% varactors functionality (i.e. $V_{C1}$=$V_{C2}$=4V) and when applying 8V to the varactors. Figures 34, 35 and 36 show the S-parameters of these two states.

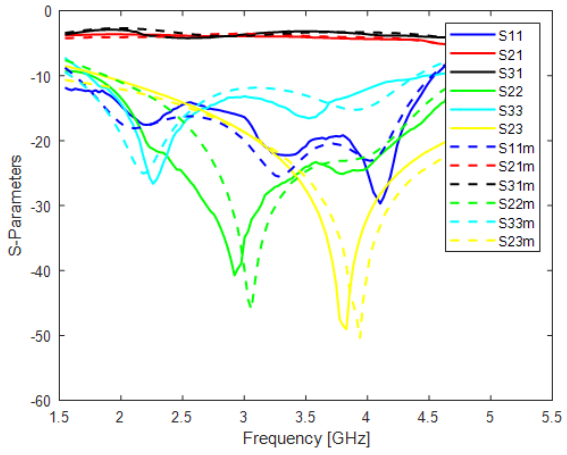



Figure 34 Simulated vs Fabricated Results when VC1=VC2=4V

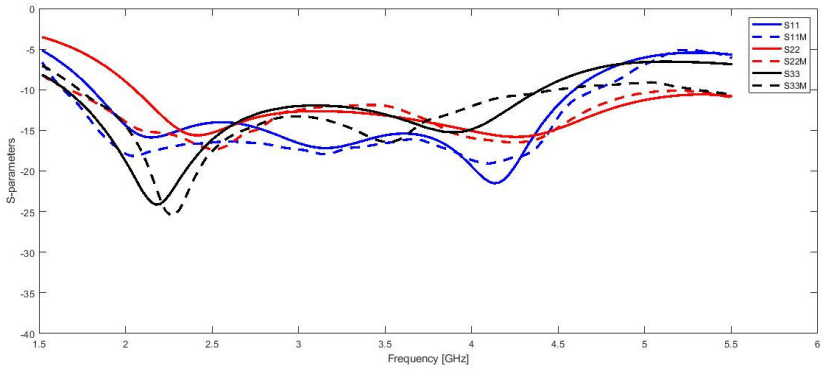



Figure 35 Reflection coefficients (simulated vs measured)

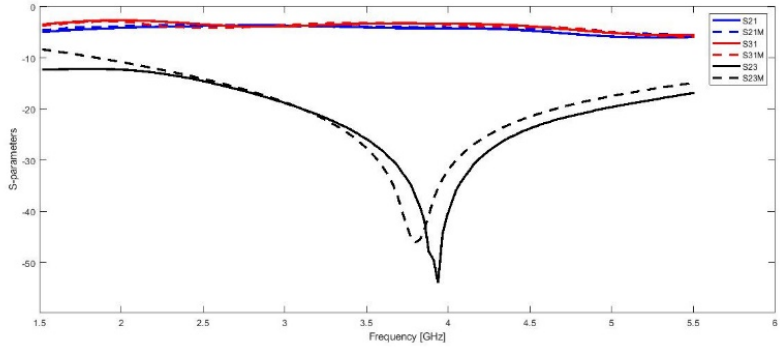



Figure 36 S21, S31 and S23 (simulated vs measured) when 8V applied

For the different states, the S-parameters showed good agreement, along the operational bandwidth, between the simulation and the measurement. A small deviation occurred because of the non-linear behavior of the active components and due to the parasitic effects of the lumped elements used in the biasing networks.

Concerning the phase difference or the phase shift at the output ports of the proposed design, some states were plotted in Figure 37 that illustrates the phase difference between the 2 outputs when supplying various voltages to the varactors. The phase of S21 and S31, at each state, were measured and then subtracted, in order to get the phase shift at the output.

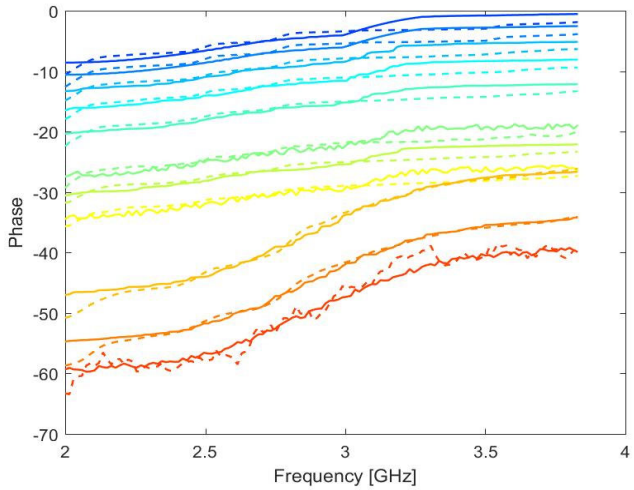



Figure 37 Phase difference upon supplying different voltage combinations

Each curve, in Figure 37, represents a different combination of varactors voltage supplied. When 0V is supplied to both varactors, the in-phase component is achieved with a deviation of maximum 7 degrees (between 2 and 3 GHz), due to parasitic effects. When the voltage applied starts changing, the phase difference changes to achieve an average of 55 degrees. It is noted that the phase variation remains linear when switching between the different states until the varactors get into their saturation state. This justifies the non-linear behavior for the states having a supplied voltage greater than 6 V, as shown in figure 37.

Table 2 represents a comparison between the out-of-phase tunable power divider presented in this work and other relevant structures.

Table 2 Comparison With Relevant Previous Designs

| References | I/O of phase | Variable phase | RL (dB) | IL (dB) | Size (mm) |
|---|---|---|---|---|---|
| [29] | In and Out | NO | >10 | 0.6-1.5 | 60x40 |
| [30] | In and Out | NO | >10 | 0.8-2.2 | 32.4x25.9 |
| [31] | Out | NO | >10 | 0.5 | 30x60 |
| [32] | Out | NO | >20 | 0.5-1 | 56.43x26.31 |
| This work | In and Out | YES | >12 | 0.3-0.9 | 40x20 |

### 4.3. The Directional Coupler

A Directional Coupler is a Four-Port Network. Directional couplers are passive microwave components that divide and distribute power while adding a phase difference between the coupled signals. Couplers are used in dividers, combiners, attenuators, filters, phase shifters, discriminators, balanced and double-balanced mixers, balanced amplifiers, and feeding networks in antenna arrays. [4] [12]

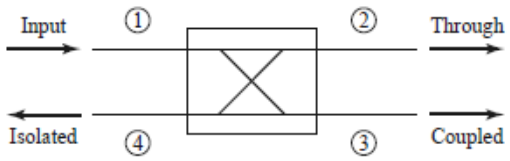



Figure 38 Directional coupler symbol [4]

Figure 38 shows the diagram of a directional coupler. Power supplied to port 1 is coupled to port 3 (called the *coupled* port) with a coupling factor $|S_{13}|^2$. However, the remainder of the input power is delivered to port 2 (the *through* port) with the coefficient

$|S_{12}|^2 = 1 - |S_{13}|^2$ (25). In an ideal directional coupler, no power is delivered to port 4 (the *isolated* port).

A special case is the 3-dB directional coupler (hybrid coupler) where the signals at the two output ports are equal [4]. A directional coupler is often used for sampling a small portion of the signal power [4]. It is used to separate between the incident signal and the reflected signal when implemented in a VNA.

There are some specifications to take into consideration when designing a directional coupler:

- Coupling C is the ratio of the coupled output power to the input power, in dB, and it is the primary specification of a directional coupler:
    - Coupling = $C = 10 \log \frac{P1}{P3}$ (26)
- Isolation I: Is the measure of the power delivered to the uncoupled port:
    - $I = 10 \log \frac{P1}{P4}$ (27)
- Directivity D: Is the measure of the coupler's ability to separate forward and backward wave components:
    - $D = 10 \log \frac{P3}{P4} = I - C$ [4] (28)

### *4.3.1. Design of a directional coupler*

In order to validate such theoretical aspects, a directional coupler has been designed as shown in Figure 39. This design is based on the simple structure of the directional coupler. The coupler was designed to have a directivity of around 25 dB. This directivity is calculated using equation (28). Figure 40 shows the coupling and isolation factors of this design.

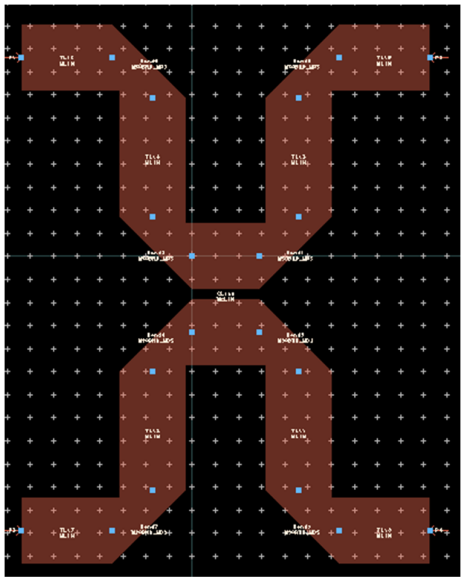


Figure 39 Our directional Coupler layout on ADS

Figure 40 represents the simulated results of the designed coupler. The results show that this directional coupler has a coupling range of -37 to -20 dB, and an isolation range of -50 to approximately -35dB.

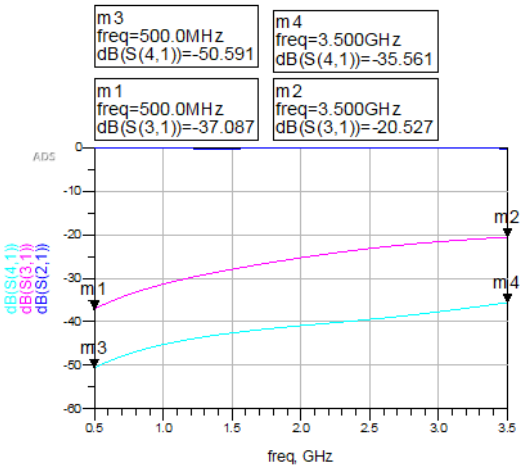



Figure 40 Results of the DC simulation

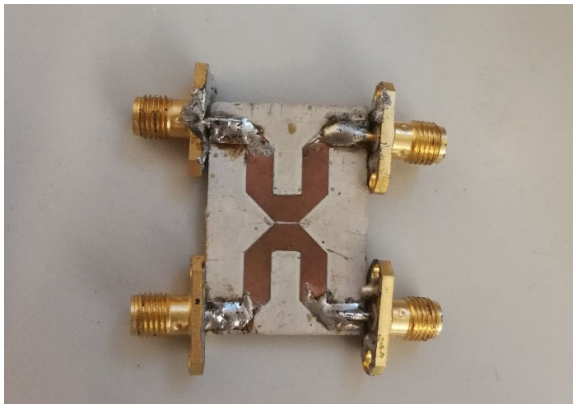


Figure 41 The fabricated prototype of the DC

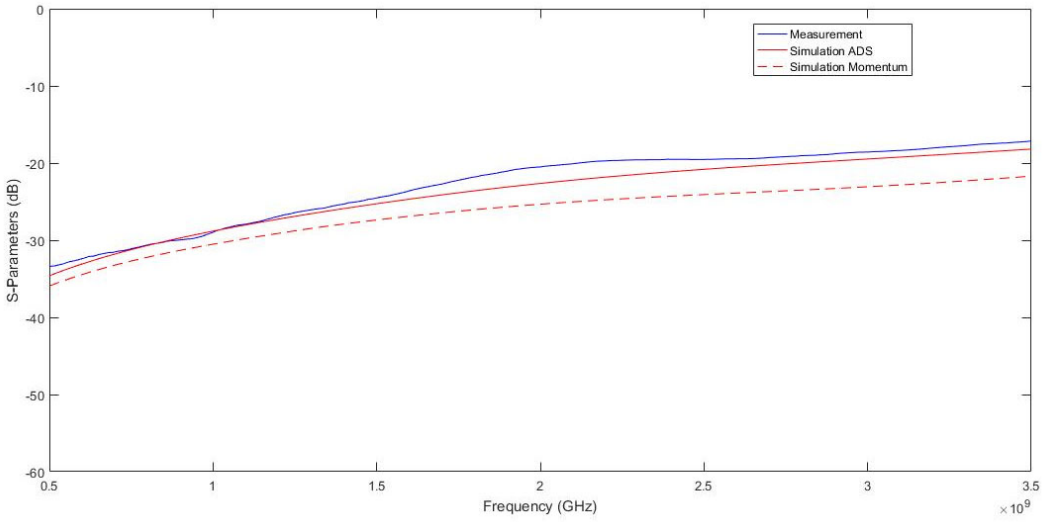



Figure 42. Measurement versus simulation results of our DC

Figure 41 shows the fabricated prototype of the designed directional coupler which was shown in Figure 39. Figure 42 shows the measured results of the fabricated directional coupler, whose layout is in Figure 39, versus the simulated ones. It's clear that the measured results match the simulated ones.

## 4.4. Mixers

### *4.4.1. Introduction to the mixer*

A mixer is mainly a passive 3-port RF device. It is used as a multiplier in RF circuits. It takes 2 inputs, which are the RF and the LO signals, and mixes them. By mixing, it is meant that it either down-converts or up-converts the frequencies. It is a critical component to design because of its nonlinear performance. The majority of mixers are composed of passive diodes, baluns and FET transistors [14].

To better understand the functionality of mixers, the following equations are used internally in a mixer in order to manipulate the signals arriving and leaving the mixer's ports.

$v_{LO}(t) = A_{LO} * \cos 2\pi * f_{LO} * t$ (29)

$v_{RF}(t) = a(t) * \cos( 2\pi * f_{RF} * \phi(t) )$ (30)

➔ $v_{IF}(t) = K * v_{RF}(t) * v_{LO}(t)$ (31)

➔ $= K * \cos(\omega RF(t)) * \cos(\omega LO(t))$ (32)

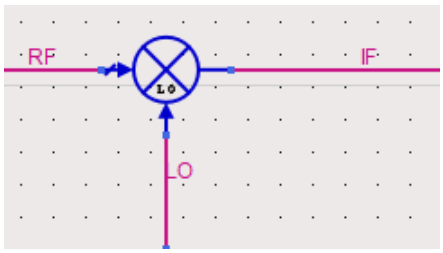



Figure 43. Mixer ports

$$v_{IF}(t) = \frac{K * A_{LO}}{2} a(t) [\cos(\omega_{RF} - \omega_{LO})t + \phi(t)] + \frac{K * A_{LO}}{2} a(t) [\cos(\omega_{RF} + \omega_{LO})t + \phi(t)] \quad (33)$$

Equation (33) shows that the mixer provides two frequencies, and depending on the application (whether it was for down-conversion or up-conversion), the option of keeping one frequency is taken and the other frequency is filtered out. [15]

The IF output signal has a smaller magnitude than the input signals, However, the information can still be demodulated and read as it was initially sent.

So when a mixer is used for frequency down-conversion, $V_{IF}$ must exhibit the following form:

$$v_{IF}(t) = \frac{K*A_{LO}}{2} a(t) [\cos (\omega_{RF} - \omega_{LO})t + \phi(t)] \quad (34)$$

In order to have the highest IF power value, $A_{LO}$ must be as large as possible. However, the LO power is the maximum power level that the LO port of the mixer can support, exceeding this limit will lead the port to be saturated and increasing more the LO power does not result in increasing the IF output power.

The mixer exhibits a conversion loss, which is the inverse of the gain. It is expressed by the following equation:

$$CL\ (dB) = -10 \log \left( \frac{P_{RF}}{P_{IF}} \right) \quad (35)$$

This conversion loss should be very low.

$$\rightarrow P_{IF}\ (dBm) = P_{RF}\ (dBm) - CL\ (dB) \quad (36)$$

Another important characteristic of a mixer is the 1dB compression point, which is the point where the conversion loss appears to be 1 dB greater than the normal value.

$$\rightarrow P_{IF}\ (dBm) = P_{RF}\ (dBm) - CL\ (dB) - 1dB \quad (37)$$

Therefore, the power at the 1dB compression point is the maximum power of a mixer.

A final characteristic, of mixers, is the isolation. After mixing the RF and LO signals, IF signals having the same frequencies as the RF and LO appear at the output.

Such signals leak across the mixer and are coupled directly to the IF output port. These signals have the same frequencies as the RF and LO frequencies, but smaller magnitudes. The leaked signal will be smaller than the incident RF power by the RF isolation value [15].

➔RF power (dBm) - Isolation (dB) = IF power (dBm) (38)

### *4.4.2. Design of a mixer*

In order to validate all the design requirements and characteristics of a mixer, a mixer with an output IF frequency of 1 MHz is designed. The mixer consists of a hybrid coupler followed by a low pass filter. The 2 input ports of hybrid coupler are fed by two signals, which have a frequency difference of 1 MHz. Then, the output signal will pass through a low pass filter to suppress harmonics and only keep the 1 MHz signal in order to get the IF needed signals.

Figure 44 shows the design of the mixer as it was executed in Keysight's ADS [11]. The fabricated prototype is shown in Figure 45.

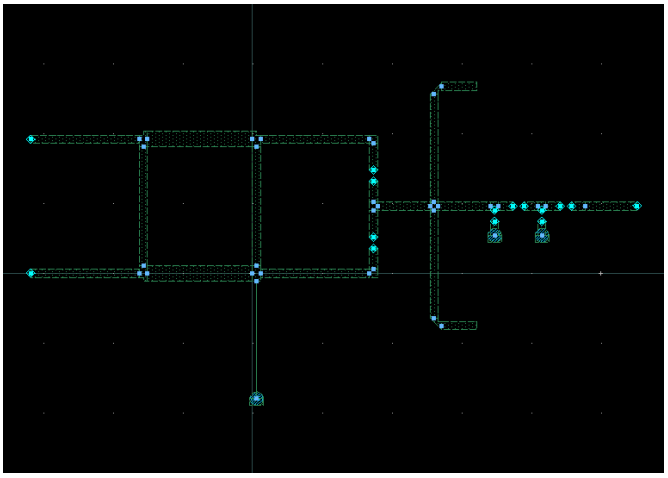


Figure 44 Layout of the mixer on ADS

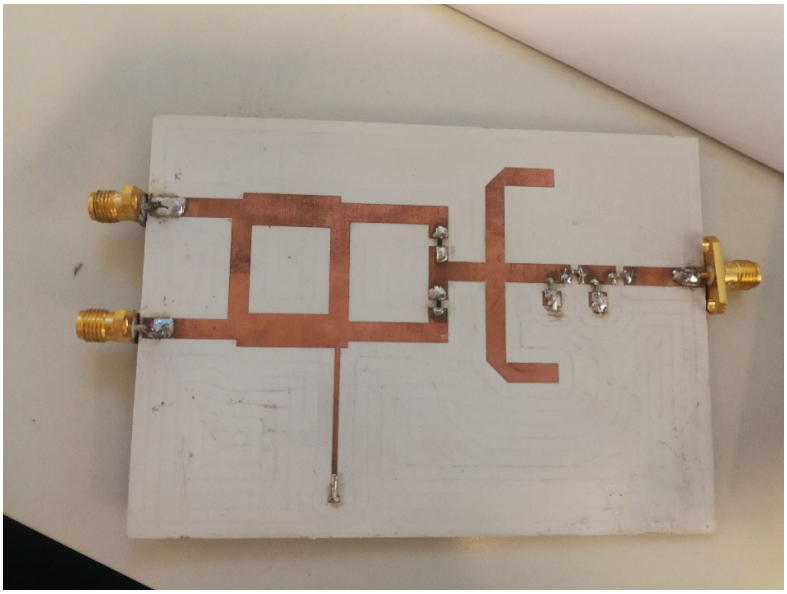


Figure 45 The Fabricated mixer

## 4.5. Amplifiers

A LNA (Low Noise Amplifier) is an active device that takes an input signal and reproduces it at the output with a larger magnitude, without changing the input signal. It is mainly a 2-port device, consisting of an input port and an output port. [17]

### *4.5.1. Introduction to the LNA*

There are many key specifications for a LNA. Such are:

- Gain and gain flatness (dB)
- Operating frequency range and bandwidth (Hz)
- Output power (dBm)
- Power supply requirements (V and A)
- Input and output reflection coefficients (VSWR)
- Noise figure (in dB) [14]

- 1 dB compression point which is the output power level where the amplifier gets into compression and starts providing distortion and harmonics, i.e. acting as a non-linear device having a decreased gain of 1 dB from its desired gain value.

As the amplifier is a two-port device, it has a 2x2 scattering parameters matrix:

$$S=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (39)$$

To insure maximum power transfer, the input and output ports must be matched:

$$S_{11}=S_{22}=0 \quad (40)$$

The gain, which is an important parameter of the amplifiers, is represented by $S_{21}$.

If the load connected to the output of the amplifier is matched, then:

$$P_o=|S_{21}|^2 P_i \quad (41)$$

$$\rightarrow G=|S_{21}|^2=\frac{P_o}{P_i} \quad (42)$$

➔ G must be greater than 1 in order to amplify an input signal.

$$\rightarrow G\ (dB) = 10 \log_{10} (G)\ [13] \quad (43)$$

They are directional, not reciprocal; so ideally $S_{12}$ =0. (44)

Low noise amplifiers (LNA) consist of a transistor, an input matching network, an output matching network, and a DC biasing network. These networks are very important to reduce reflections and improve the power flow from the input to the output ports. [18]

Figure 46 shows the circuit diagram of an LNA amplifier [18].

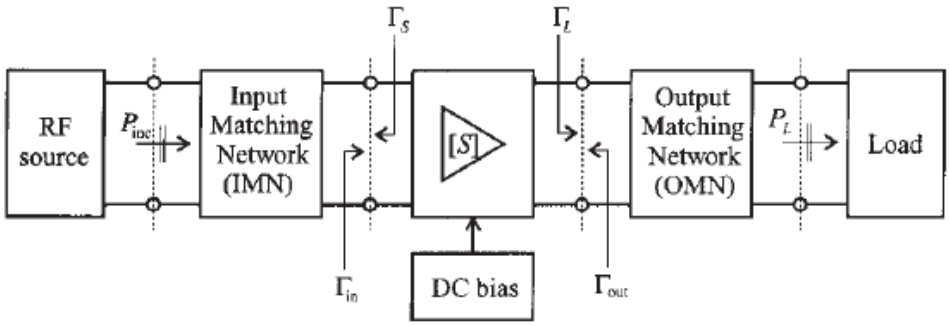



Figure 46 RF amplifier system [18]

### *4.5.2. Fabrication of a LNA*

A LNA is used in this work with Figure 47 illustrating its layout. The circuit, in Figure 47, consists of an amplifier IC connected to a biasing network.

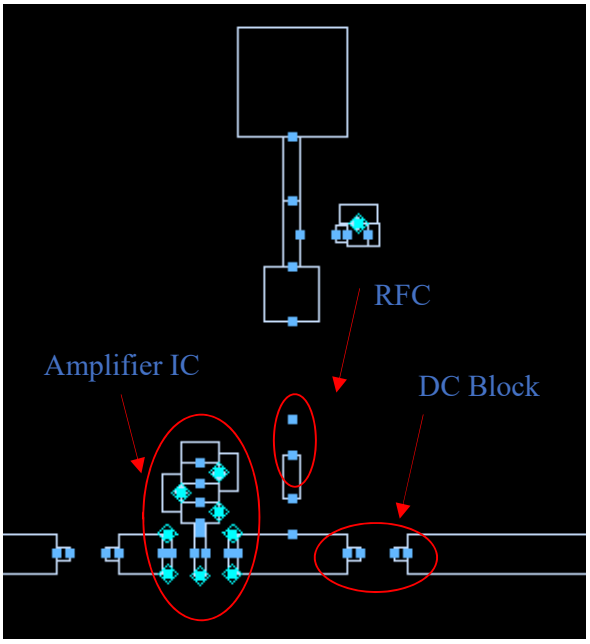



Figure 47 Layout of the amplifier

The amplifier IC used has 3 pins: input, ground and output. The amplifier in placed in series with the circuit. The signal is incident at the input pin first and then gets transmitted to the output port with a specific gain. This gain is defined when the amplifier is designed.  At its input and output pins, capacitors are added to block the DC from interfering with the RF circuit signals.

However, an RFC (RF choke), which is an inductor, is used to block the RF from going to the DC biasing network.

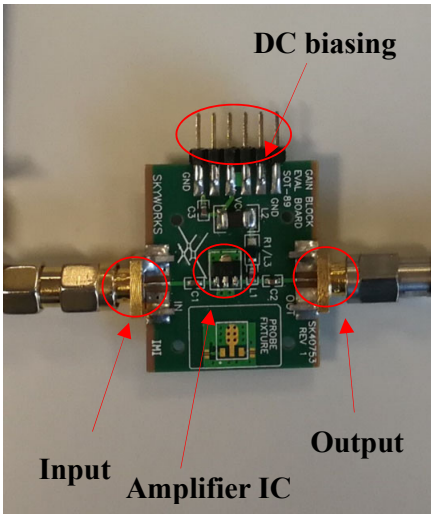



Figure 48 Evaluation board of an amplifier

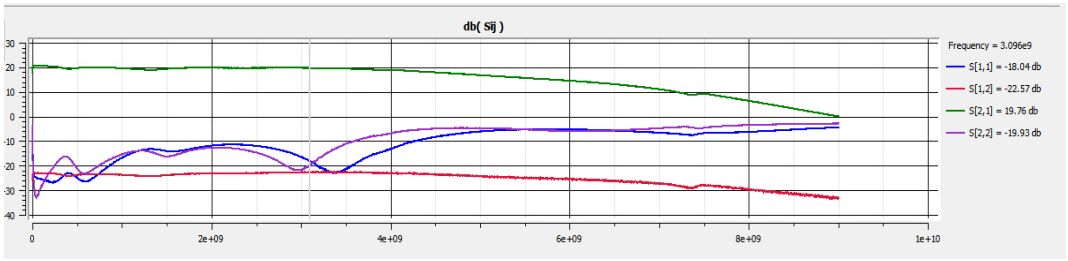



Figure 49 Measured results of the amplifier

In Figure 49, the measured results of the amplifier are shown. It is clear that it has a gain of, approximately, 20 dB over the bandwidth from 0 to 4.2 GHz.

### 4.6. Attenuators

An attenuator is a passive RF component that is used to attenuate/weaken the power coming from one input into the output. It doesn't require any extra DC biasing in order to operate. It is a reciprocal device and the signal can cross through its two ports (forward and backward).

The attenuation level is expressed in decibels (dB) and it is equal to:

$$A = 10 \times \log_{10}(\frac{Pi}{Po}) \qquad (45)$$

Pi (Π) and T-section attenuators are the most commonly used attenuator configurations. In this work, a T section is designed and fabricated as shown in Figure 50. The attenuator is measured as shown in Figure 51.

Figure 50 A -10 dB attenuator

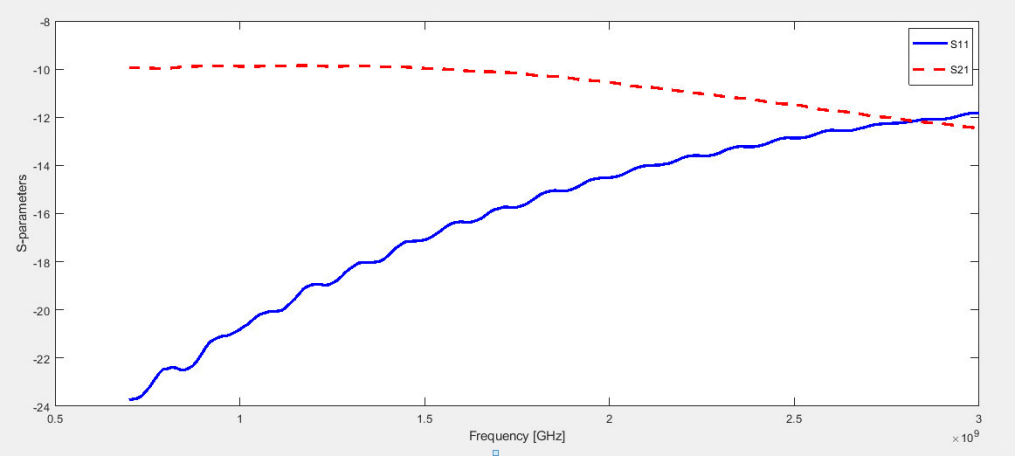



Figure 51 Measured Results of the attenuator

This attenuator has a 10 dB attenuation level and is designed using resistors. The values of the resistors are got from an attenuator calculator where the attenuation factor is inputted along with the option of choosing a Pi or T section topology.

## 4.7. Filters

Filters are devices that process a signal with a frequency-dependent way (i.e. their functionality depends on the signal's frequency). Filters are used when an application requires signals with specific frequencies. There are many types of filters: low-pass, high-pass, band-pass and band-stop.

### *4.7.1. Different types of a filter*

A low-pass filter stabilizes an amplifier design by lowering its gain at high frequencies, which may cause oscillations due to the high phase shift at these high frequencies. A frequency $f_0$ determines the threshold frequency, or the maximum

frequency, that is allowed to pass through the filter, and every frequency that is higher than this $f_0$ will be filtered out and blocked.

To block the DC offset in high gain amplifiers or other circuits, a high-pass filter is used. Such a filter has a threshold frequency $f_0$ that determines the minimum frequency that can pass through the filter. [20]

A band-pass filter passes the signals within a frequency bandwidth $\Delta\omega$, and blocks the ones at all frequencies outside this bandwidth.
It has a fundamental frequency, which is denoted by $\omega_0$ and defines the center frequency of the filter bandwidth. [21]

Filters are used to separate the incoming signals. They let the signals of interest pass and attenuate the unwanted frequencies.

Filters also help smooth waveforms by eliminating harmonics and restricting the signals at the output of a D /A system [20].

### *4.7.2. Design of a bandpass filter*

In this report, a 1MHz band-pass filter is needed to let the IF output signal, which is at 1MHz, pass and block other frequencies.
Figure 50 shows the layout of the fabricated 1 MHz filter in ADS. An IC, with appropriate biasing and RF chokes and dc blocking capacitors incorporation, was used accordingly. Figure 51 shows the fabricated circuit on an FR4 board.

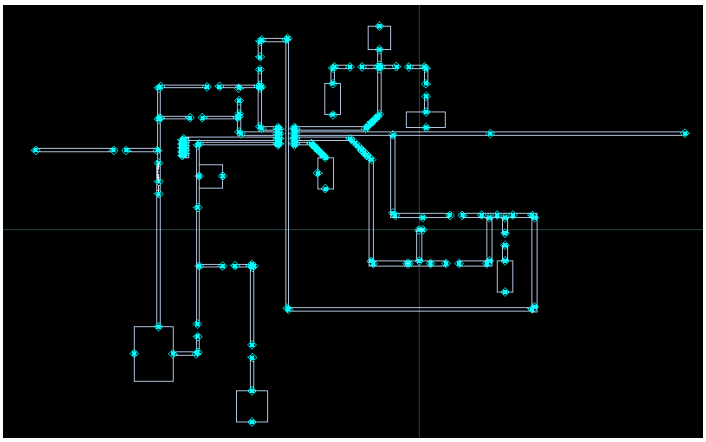


Figure 52 Layout of our designed 1MHz filter done on ADS

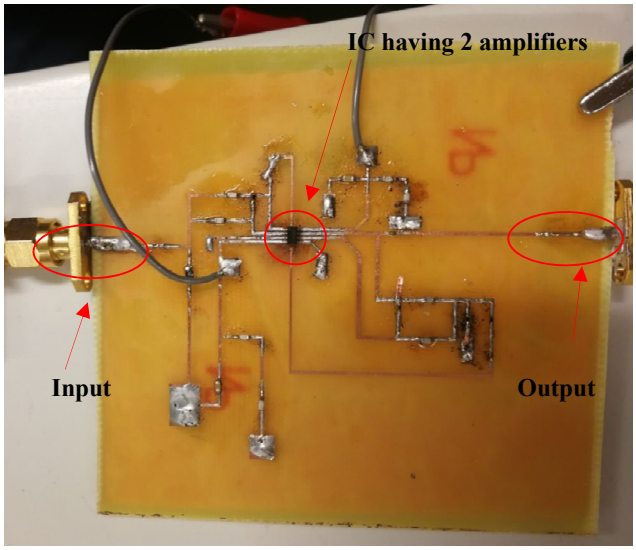



Figure 53 Our Fabricated and Soldered 1MHz filter

## 4.8. VNA Assembly

### *4.8.1. Assembling the VNA components*

To assemble the VNA, the above components are combined. An RF source is applied to one port of the VNA. Another source, mainly the LO, is applied to the other

side of the circuit. These sources are provided using a frequency synthesizer (Valon 5009) [34] to sweep the frequency within the desired range. The frequency synthesizer should be programmed to provide the needed frequencies and amplitudes at a constant time Δt. After applying these sources, their outputs will be mixed to generate an IF output at 1MHz. For the case of a 1-port VNA, 2 IF outputs are generated ($a_1$, $b_1$), whereas for the 2-port VNA, 4 IF outputs are generated ($a_1$, $b_1$, $a_2$, $b_2$). As a proof of concept, a simulation is conducted in ADS [11], and the $S_{11}$ results are compared with the $S_{11}$ measured results of a compact VNA.

Figure 54 shows the compared results. The first plot is the magnitude and the second one is the phase of the DUT which is a BPF.

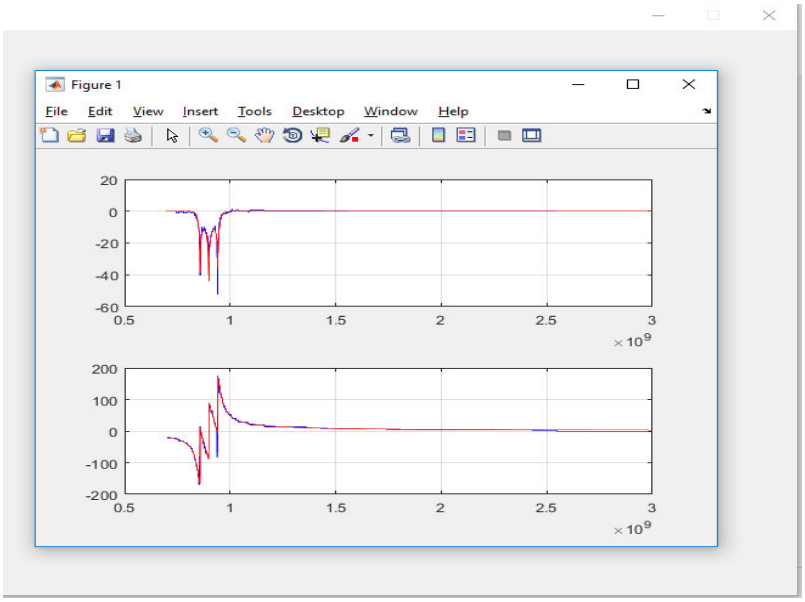



Figure 54 S11 of the simulation vs the compact VNA

The layout of a 1-port VNA built using ADS, is shown in Figure 55:

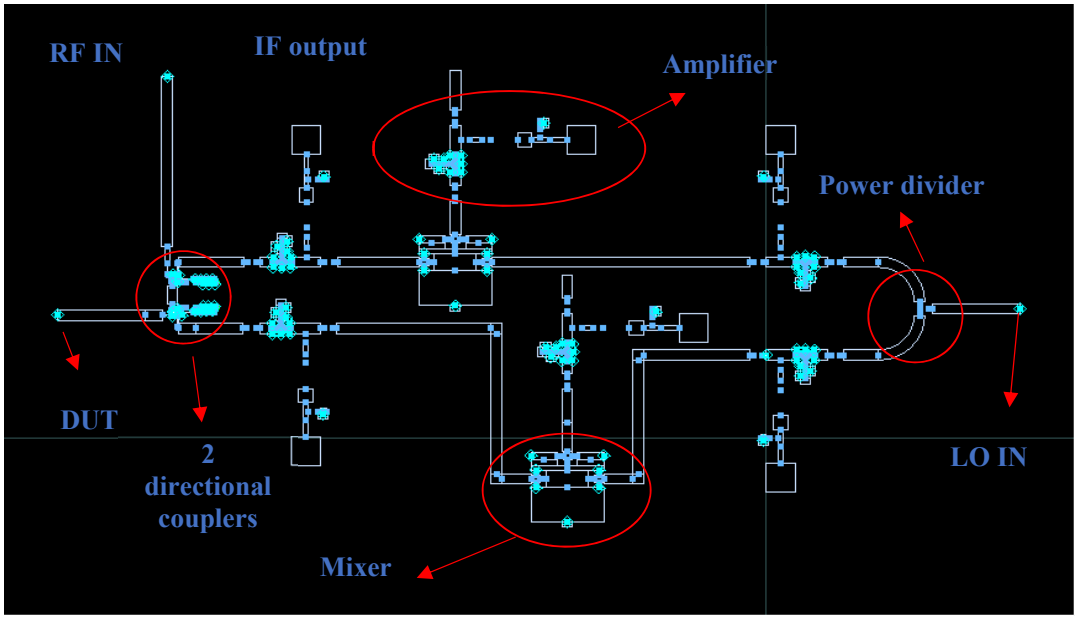



Figure 55 Layout of a 1-port VNA

Moreover, a 1-port VNA is assembled and tested. However, due Data Acquisition devices limitation at 1MHz, a down-conversion method is applied to down-convert 1 MHz to around 1.9 kHz. This process is done using an Analog multiplier IC [22].

The outputs of the VNA are connected to a 1MHz bandpass filter and followed by an analog multiplier, which down-converts the 1 MHz frequency signals, as shown in Figures 52 and 53. A 1.9 kHz bandpass filter is then incorporated, as shown in Figure 53, to process the down-converted signals.

Figure 56 shows the different RF components assembled to form a VNA.

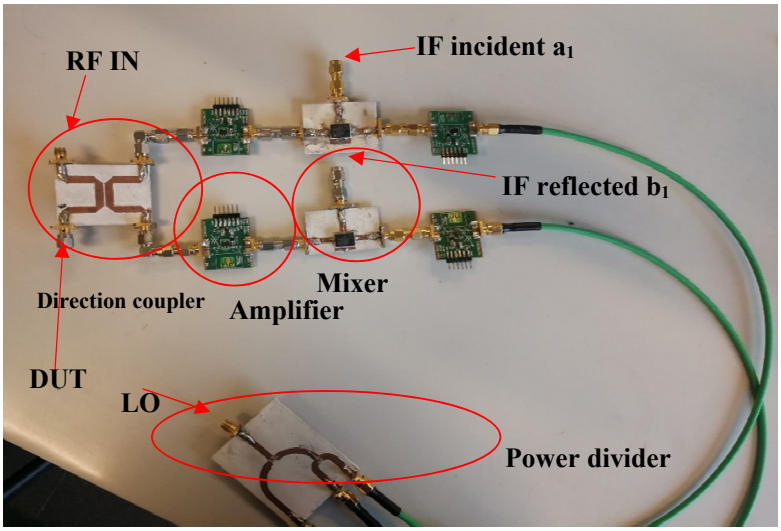



Figure 56 Assembled VNA components

### *4.8.2. Design of an analog multiplier*

Figure 57 shows the schematic of the AD633 IC, which consists of 3 operational amplifiers connected through summation and multiplication tools.

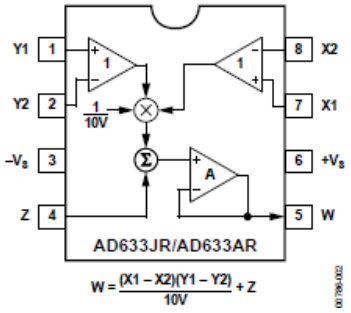



Figure 57 Analog Multiplier IC [22]

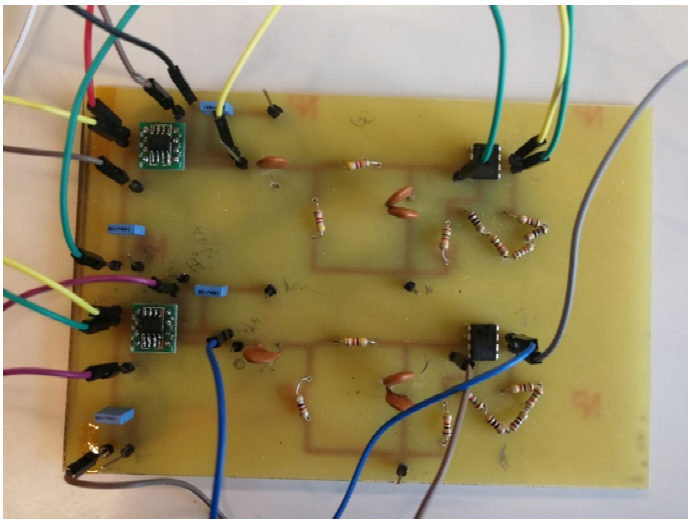


Figure 58 Fabricated Analog multiplier with a 1.9 kHz filter

This analog multiplier circuit is responsible of down-converting the 1 MHz IF output signal to around 1.9 kHz by applying 2 inputs to it. The first one is the output of the VNA and the second one is a signal from an external LO. These 2 signals should have a frequency difference Δf of 1.9 kHz. This analog multiplier is followed by an active 1.9 kHz filter to account for the attenuation the analog multiplier does, as shown in Figure 53. The attenuation done is equal to $\frac{E_1 * E_2}{10}$, where $E_1$ and $E_2$ are the magnitudes of the 2 input signals.

After this stage, a Data Acquisition device simultaneously reads and saves these down-converted IF outputs. This device should be synchronized with the frequency synthesizer that increments the frequencies of the RF and LO by 1 MHz every Δt to cover the whole frequency range needed and allow the data acquisition unit to read and save the IF outputs at each Δt.

### *4.8.3. Data Acquisition*

A Data Acquisition device is used, at this stage, which consists of the DAQ combined with the labView software [33] to extract the data from the VNA.
The collected data (IF signals from the VNA) are first used to perform the VNA calibration, by connecting an open, short, load to the VNA, then a DUT will be connected to get its S parameters. [23]

# CHAPTER 5

# CALIBRATION TECHNIQUES

The accuracy of the measured S-parameters depends on the load port termination and matching. Any mismatch or improper load termination results in having the incident output signals ($a_1$ and $a_2$) not equal to zero and this leads to a violation to the definition of the S-parameters. [24]

Sometimes, when connecting a DUT to the DUT port of the VNA, it happens that this DUT doesn't have a perfect matching and this will lead to some errors. These errors should be accounted for in calculating the S-parameters of the DUT [25]. As a result, calibration is essential in order to account for such errors between the source and the load.

## 5.1 Error types

There are many types of errors. One type is the systematic error, which is due to the imperfection of the VNA and the setup. They are predictable and can be mathematically removed during the measurements. [2]

However, another type is the random errors. These errors randomly vary with time and they are unpredictable. They are due to the DUT noise. Such errors cannot be removed by calibration.

A third type is the drift errors, which are due to the system w they are created after calibration. This error type is mainly caused by the variation of the temperature and it can be removed by further calibration. [2]

### *5.1.1 Systematic errors*

In a two-port VNA, there are 12 errors to be taken into consideration. Some of these errors are related to the directivity and the crosstalk of the signals. Such errors fall are under the signal leakage class. Other errors are related to the source and load matching and they fall under the reflection class. A third class relates to the transmission and reflection tracking errors. [2] [26]

These 3 classes are valid for the forward direction and the same are present in the reverse direction, which lead to a total of 12 possible errors. Whereas for a 1-port VNA, only 3 error terms are present; which are the directivity, source match and reflection tracking.

## 5.2 What is a Vector-Error Correction?

It is a way to characterize the systematic errors by measuring the known calibration standards and then removing their effect. The calibration standards are the Open-Short-Load (OSL) standard for a 1-port VNA, and Open-Short-Load-Through (OSLT) standard for a 2-port VNA.

The OSL standard removes the 3 error terms of the 1-port VNA whereas the OSLT standard removes the 12 error terms of the 2-port VNA.

In order to achieve these standards, a calibration kit is used.

The VNA should mainly have some definitions for some calibration kit types. Any calibration kit used should have its cal-kit definition file stored in the memory of the VNA.

Thus, if a new calibration kit standard is used, its information shall be entered and stored in the VNA in order to be considered as a proper calibration. [26]

### 5.3 VNA Error Correction

For the 1-port VNA, 3 systematic error terms exist. Hence, 3 equations with 3 unknowns should be created and solved to get these 3 error terms: $E_{RF}$, $E_{RF}$, $E_{DF}$. These 3 terms are related to the error due to source matching, reflection tracking and directivity, respectively. These 3 equations are solved by using the calibration standards of a calibration kit; for example: Open-Short-Load.

After getting these 3 terms, an equation combines them to calculate and get the actual $S_{11}$ of a 1-port component.

It is feasible to get the $S_{11}$ of a 2-port device, using the 1-port error correction method, by terminating the second port with a perfectly matched load. If the second port is not properly matched, the calibration will not be accurate and a 2-port calibration should be done instead. So in order to get the $S_{11}$ actual, equation 35 is used:

$$S_{11M} = E_{DF} + E_{RF} * \left( \frac{S_{11A}}{1 - S_{11A} E_{SF}} \right) \qquad (46)$$

Where:

- $E_{DF}$ is the error of the directivity
- $E_{RF}$ is the error of the reflection tracking
- $E_{SF}$ is the source match
- $S_{11M}$ is the measured reflection coefficient without taking the calibration errors into consideration and it is equal to $\frac{a_1}{b_1}$
- $S_{11A}$ is the actual reflection coefficient, while taking into account the errors

If a 1-port calibration is not correctly done, or not done at all, ripples will be created to interfere with the measured signal. In this case, the measured $S_{11}$ will not be considered accurate nor correct. Such measured signal cannot represent the actual

component's reflection performance. [26]. An example of such effect is shown in Fig. 57 [26].

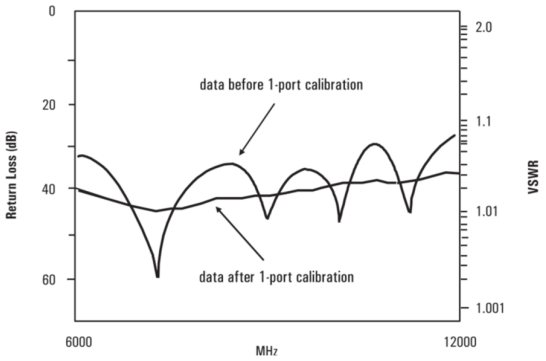



Figure 59. Difference between calibrating and not calibrating [26]

Concerning the 2-port calibration, it is more accurate than the 1-port calibration. It takes into account all the systematic errors, which are the 12 error terms: $E_{SF}$, $E_{RF}$, $E_{DF}$, $E_{SR}$, $E_{RR}$, $E_{DR}$, $E_{XF}$, $E_{XR}$, $E_{TF}$, $E_{TR}$, $E_{LF}$, $E_{LR}$.

Where:

- $E_{DF}$ is the error of the directivity in the forward direction
- $E_{RF}$ is the error of the reflection tracking in the forward direction
- $E_{SF}$ is the error of the source match in the forward direction
- $E_{DR}$ is the error of the directivity in the reverse direction
- $E_{RR}$ is the error of the reflection tracking in the reverse direction
- $E_{SR}$ is the error of the source match in the reverse direction
- $E_{XF}$ is the error of the leakage in the forward direction
- $E_{XR}$ is the error of the leakage in the reverse direction
- $E_{TF}$ is the error of the transmission tracking the forward direction
- $E_{TR}$ is the error of the transmission tracking the reverse direction

- $E_{LF}$ is the error of the load match in the forward direction
- $E_{LR}$ is the error of the load match in the reverse direction

As a result, 12 equations with 12 unknowns are solved to get these 12 error terms. After getting them, the S-parameters will be calculated and provided. Each S-parameter is a function of the calculated errors and all the measured S-parameters.

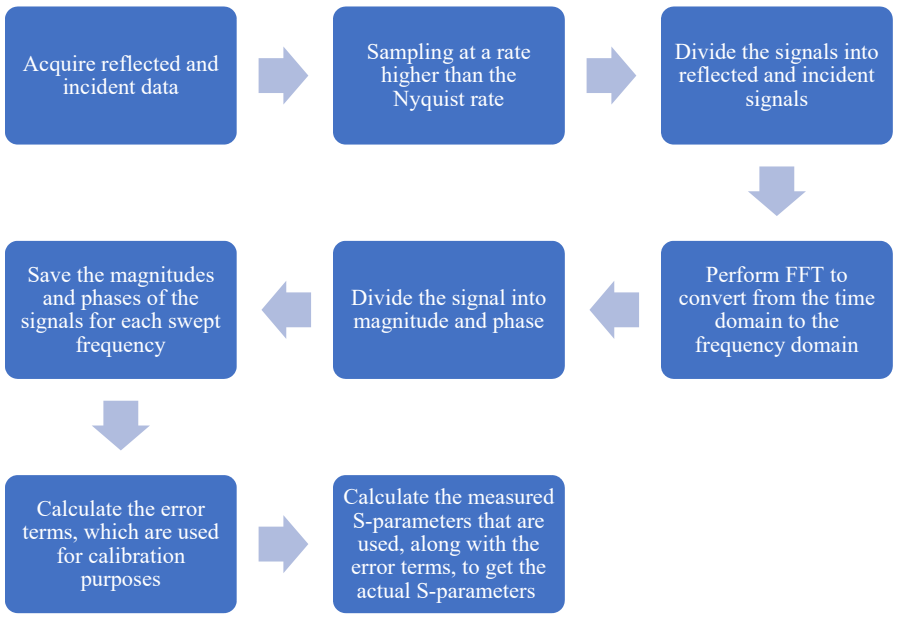
# CHAPTER 6

# EXTRACTING THE S-PARAMETERS FROM THE VNA

After assembling the VNA system, a software block is implemented in order to extract and save the down-converted IF signals that contain the replicas of the incident and reflected signals. This extracted data is used for calibration in order to overcome the errors described in chapter5. The ratio of the $a_s$ and $b_s$ is used to get the measured S-parameters, which are combined with the error terms, to calculate the actual S-parameters.

This software block behaves as an Analog-to-digital converter in order to acquire, save, and process data. The used device is the DAQ (Data Acquisition), which is compatible with LabView [37].

The process follows the following flow chart:



1. Acquire the data, of the different paths (reflected path and incident path), simultaneously
2. Sampling the data at a rate higher than the Nyquist rate.
3. Divide the signals into reflected and incident signals
4. Perform Fast Fourier Transform (FFT) on the signals to convert them from the time domain to the frequency domain.
5. Divide the signal, after performing the FFT, into magnitude and phase
6. Save the magnitudes and phases of the signals of each swept frequency
7. Process these data by a Matlab code in order to calculate the error terms, which are used for calibration purposes, and to calculate the measured S-parameters that are used, along with the error terms, to get the actual S-parameters.

It is important to note that the signals arriving to the DAQ should have acceptable magnitudes and frequencies so that they can be read by the DAQ. The software execution of this flow chart is beyond the scope of this work and hence, will not be detailed herein.

# CHAPTER 7

# CONCLUSION AND FUTURE WORK

In this work, a 1-port VNA is assembled using the different needed microwave components. However, the main novel aspect and focus of this thesis is on the design of phase-tunable power divider that was detailed in chapter 4.

In this work, a new compact power divider, that operates as an in-phase and variable out-of-phase, was proposed, fabricated and measured. It is the first design that has in-phase and variable out-of-phase states, simultaneously, along with a compact size while using a minimum number of active components.

The structure was designed using the microstrip line theory along with integrating two varactors and their biasing networks. An infinity shape was connected also as a meandering and multistage technique to enhance the matching of the ports.

These varactors were used to deliver a variable phase shift between the 2 output ports. So, the design was simulated first, then in order to validate the results, the prototype was fabricated and measured. Upon supplying different voltages to the varactors, the phase shift was varying between 0 and 55 degrees, while maintaining a return loss better than 12 dB and an insertion loss between 0.3 and 0.9 dB, over the operational bandwidth (2- 3.8 GHz).

Future directions of this work can relate to fully developing a software controlled two-port miniature VNA that can be integrated within multiple portable devices. Such a device, not only advances measurement techniques but drives new sensing innovations and explores new possibility in microwave designs, adding that wider tunable power divider can be developed to be used in new various applications.

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