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WIDEBAND POWER AMPLIFIER DESIGN WITH A HIGH DRAIN EFFICIENCY

by
MOHAMAD YEHYA NASSAR

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First and foremost, praises and thanks to ALLAH, the Almighty, for His blessings throughout my research work to complete my thesis successfully.

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ABSTRACT
OF THE THESIS OF

Mohamad Yehay Nassar for Master of Engineer
Major: Electrical and Computer Engineering

Title: Wideband Power Amplifier Design with a High Drain Efficiency

This thesis presents an optimized, broadband, Doherty-based amplifier that employs an unequal power split between the main transistor and the six-auxiliary transistors. Different unequal power splits are adopted to optimize the output power and enhance the back-off power (BOP) level efficiency of the amplifier in comparison to an equal power splitting topology. The amplifier operates at a bandwidth of 2 GHz with a (BOP) of 8 dB, drain efficiency greater than 40%, and a fractional bandwidth of 100%. We tested the final optimized design at the LAB using a driver amplifier, signal generator, and spectrum analyzer. The input radio frequency (RF) signal is a continues-wave (CW) and its frequency swept from 1.8 to 3.8 GHz. The experimental measurements show a Doherty-like efficiency behavior from 1.8-3.8 GHz. The output power is 40±3 dBm and 43.8±2.3 dBm, corresponding to 8 dB BOP and peak power levels, respectively. The measured drain efficiency is between 45%-60%, and 42%-70% respectively. The efficiency of the optimized amplifier at the BOP level is improved. Therefore, it can be used for many modern communication systems, especially for those who have a high peak to average power ration (PAPR). Also the load modulation effect of the conventional DPA is totally removed. Hence, the operating bandwidth of the amplifier is increased, which means that the amplifier can handle many signals at the same time. So a single power amplifier can be used at the base station instead of using multiple ones.

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CHAPTER I

INTRODUCTION

Power amplification of electrical signals has played a key function in electronic systems ever. Since, they were the base unit of any wireless communication system. Such a capability has facilitated the development of some of the most important electronic systems that we use on a daily basis, such as the telephone, radio, and television. In fact electrical engineers have put the details of designing robust, efficient, and stable power amplifiers (PAs), first with vacuum tubes, and then with discrete transistors [1].

RF power transistors can either function as high-resistance current sources, or as low-resistance switches, or - in some amplifiers- as a high-resistance current source during part of the "on" interval and as a low-resistance switch during another part of the "on" interval ("mixed-mode" operation).

A defining property of a PA is that its output signal power delivered to a load is larger than the input signal power. Also PA converts the DC power supplied through the DC biasing lines into output signal power. Therefore, a PA is an energy conversion circuit very much like a DC-to-DC converter or an RF oscillator, which converts DC power into constant wave (CW) power. However, unlike DC-to-DC converters or oscillators, an ideal PA converts the DC power into output signal power under the linear control of an RF input. PA is simply a DC-to-modulated-RF converter [1].

The operation of PAs is governed by two main equations can be identified as follows:

$$PE = \frac{P\_out}{P\_DC} \quad (1)$$

$$PAE = \frac{(P\_out - P\_in)}{P\_DC} \quad (2)$$

PE is the power conversion efficiency reflecting the percentage of the DC power drawn from the power supply, which has been converted into output signal power. This figure of merit is also called drain / collector efficiency. Power-added efficiency (PAE) is calculated by subtracting the input power from the output power to include the effect of the PA driver in the efficiency metric. Clearly, for large power gains, PAE approaches power efficiency (PE).

One of the most challenging in designing the PA is the nonlinearity behavior of the transistor. The designer needs to design a PA that has approximately a linear transfer function between input and output. Which means a high efficient amplifier with less harmonic and intermodulation.

Nowadays everything is controlled via internet network, so the need for communication system with high data rate to transfer a huge amount of data between the users is increased. And to achieve that a new complicated modulation schemes are adopted [2] . Consequently, the bandwidth and the peak to average power ratio of these system are increased. Hence there is an increasing demand for wideband power amplifiers (PAs) with a high efficiency in deep power back off in order to reduce the operating expenses and to improve data throughput in a given radio transceiver.

In this work we designed a PA that operate over a wideband of frequencies with a high efficiency at the BOP level. The designed amplifier is suitable for many communication standard that work at the same band of frequencies.

This thesis is organized as follows. Section 2 provides literature. Section 3 describes the steps of designing a broadband PA and the simulation results. Section 4 introduces the implementation and measurements results of the fabricated design. Finally, section 5 is the conclusion.

CHAPTER II

LITERATURE REVIEW

The design of PA with high drain efficiency at deep BOP level and wide bandwidth has been well researched. Although the literature covers a variety of such PA, this review will focus on the designs that are based on the Doherty technique. Even though, Doherty PA has the best efficiency at the BOP level but it has narrow bandwidth due to the load limitation effect. So all research is focused on mitigating the impact of this problem. For example, if the phase delay between the main and auxiliary transistor is reduced the load modulation will reduce [3]. In the other hand, an accurate calculation for the impedances of the combining network leads to a perfect matching between the two transistors and improves the total bandwidth [2]. Using N auxiliary transistors removes the load modulation effect, and provides a wide bandwidth amplifier as in [4]. These recent designs have begun to provide insight into how to improve the drain efficiency and to extend the operating bandwidth.

Although the past design have high-efficiency and wide bandwidth but we still need to improve the performance of the PA. We noticed that most of the designs use an equal power splitter at the input stage. The disadvantage of this technique that the main transistor will be under a high-compression situation. Though replacing the equal splitter by an equal power splitter could increase the overall efficiency.

The block diagram of a conventional DPA is shown in Fig. 1, where the main and auxiliary amplifiers are interconnected at the output through an impedance inverter network (IIN) and an impedance transformer network (ITN) used to match toward 50-Ω

terminations. Up to the transition point, i.e., the point that corresponds to the turning ON of the auxiliary amplifier, the impedance seen by the main amplifier is given by:

$$R_L = \beta * R_{opt} \quad (3)$$

Where R_{opt} is the required intrinsic load for the main device to deliver its peak output power and β is the load modulation factor. The auxiliary amplifier, turned ON at the transition point, provides current to the output termination and hence decreases the load seen by the main amplifier from $\beta * R_{opt}$ at the transition point to R_{opt} at peak output power. This load modulation is achieved by the IIN that is implemented as λ/4 transmission line (TL) having a characteristic impedance of

$$Z_T = Ropt. \quad (4)$$

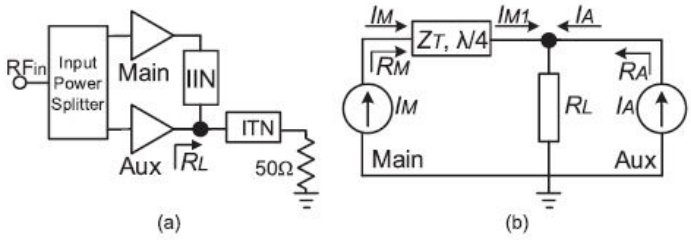


Figure 1 Conventional DPA (a) Block diagram (b) simplified equivalent circuit. Rm and RA are the load seen by the main and auxiliary amplifiers [3]

A Doherty Power Amplifier (DPA) has many limitations that reduce the bandwidth and degrade the drain efficiency. These limitations could be summarized as follows:

1. Impedance inversion at the Back-Off power level: which takes place through a $\lambda/4$ transmission line (TL) that connects the two devices. This TL is designed to operate at the center frequency. As the PAPR of the input signal increases the modulation factor β of the signal increases, and hence the

mismatch at the ends of the TL becomes greater and reduces the bandwidth of the PA [4].

2. Load modulation: This limitation is related to the fact that any matching network operates over a specific span of frequencies [4].

Based on these two drawbacks, many research studies tried to improve the performance of the DPA.

A. Improved Doherty Amplifier Design with Minimum-Phase Delay in Output Matching Network

One of the solutions to improve the performance of the DPA is to minimize the phase delays of the output matching networks (OMN) for main and auxiliary transistors. The phase delay impacts the load modulation and the operation bandwidth of the PA [3]. The function of the OMNs is to transfer the load impedance into different impedances seen by the transistors at different power regions. Fig 2 depicts this operation.

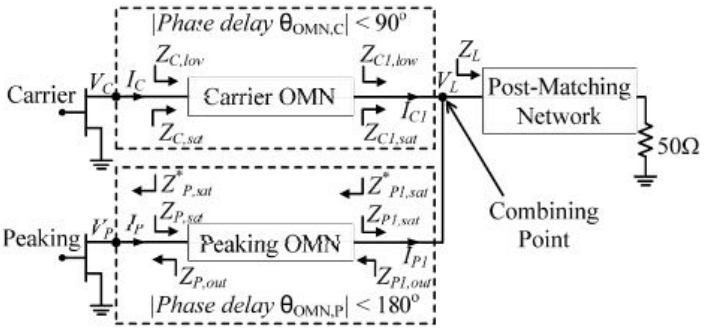


Figure 2 Simplified circuit diagram of the proposed DPA [4]

It is clear that the OMN of the carrier transfers $Z_{C1,low}$ into $Z_{C,low}$ when the transistor is in the low power region and transfer $Z_{C1,sat}$ into $Z_{C,sat}$ in the high power

region. The OMN for the auxiliary also transfers the $Z_{p1,low}, Z_{p1,sat}$ impedances into $Z_{p,low}, Z_{p,sat}$ respectively. The designer tries to recalculate the impedances of the OMN based on the S-parameter and a load pull calculation to ensure that the phase delays are as small as possible. Fig 3 depicts the fabricated design.

This design achieved a bandwidth of 600MHz with a 51-55% drain efficiency at 10dB BOP [3].

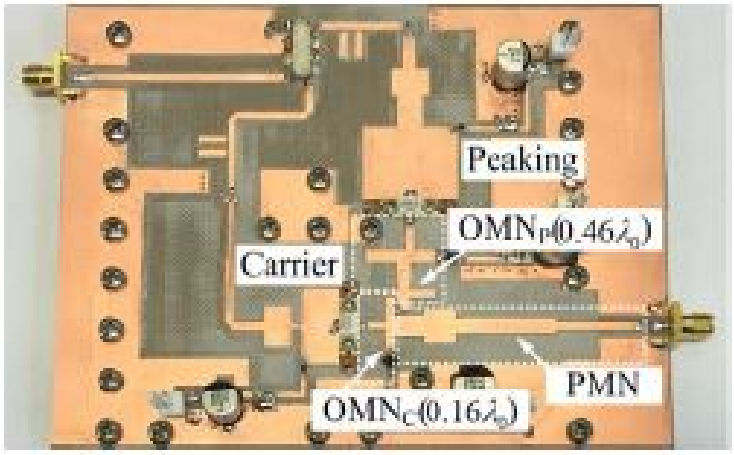


Figure 3 Photo of the fabricated DPA

B. Toward a More Generalized Doherty Power Amplifier Design for Broadband Operation

The generalized GDPA used to increase the efficiency as well as the bandwidth of the PA. In this method, the designer introduces a theoretical parameter(α) [2]. This integer parameter reduces the complexity of the output combiner network. The basic structure of the CDPA and GDPA are shown in Fig 4

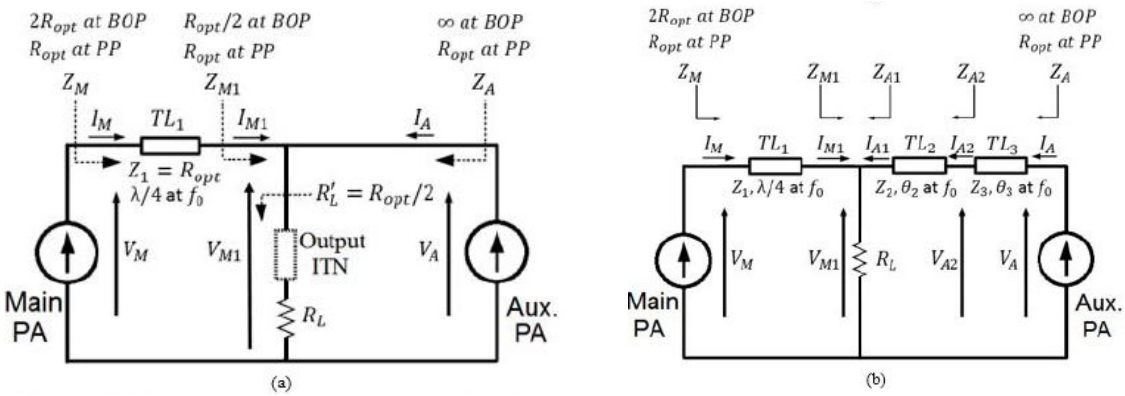


Figure 4 Basic structure of (a) CDPA (with an output ITN) and (b) generalized DPA

The inverse transmission network (ITN) is replaced by two λ/4 transmission lines (TLs) at the auxiliary branch of the DPA. The value of Z_1, Z_2, Z_3, and R_{opt} are calculated based on the value of α.

$$R_{opt} = 2\,\alpha^2 R_L \quad (5)$$

$$Z_1 = \frac{R_{opt}}{\alpha} \quad (6)$$

$$Z_2 = \frac{R_{opt}}{\alpha^{3/2}} \quad (7)$$

$$Z_2 = \frac{R_{opt}}{\alpha^{3/2}} \quad (8)$$

Fig 5 shows the photograph of the fabricated PA. GDPA provides a bandwidth of 560 MHz and a drain efficiency of about 50% at the 6 dB BOP.

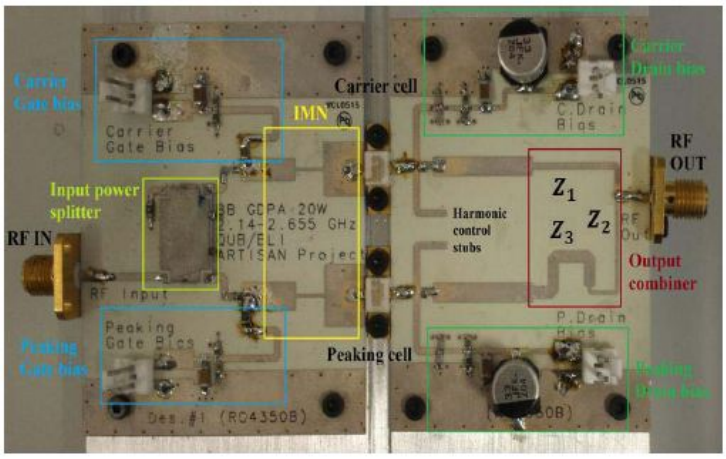


Figure 5 Photograph of the fabricated layout

C. The Influence of the Output Impedances of Peaking Power Amplifier on Broadband Doherty Amplifiers

In the traditional Doherty power amplifier DPA, the output impedance of the peaking (auxiliary) must be equal to infinity at the output Back-Off power (BOP). This can be realized at a certain operating frequency. Weimin et al. [5] have demonstrated that the peaking matching network should be added to match auxiliary PA and by tuning the output impedance toward quasi-open circuit [5]. In this study, it is shown that the output impedance of the C-class peaking transistor changes between ON and OFF states, and this change will affect the performance of the DPA especially in case of broad band application. The solution was to design a matching circuit that compensates this fluctuation in the impedance value to make sure that the peaking transistor has an infinite impedance at the BOP. The change of the output impedance of the peaking transistor is called the Load Modulation (LM). The following figure (Fig 6) depicts the fabricated DPA. This work achieves a bandwidth of 1 GHz (1.7-2.7 GHz) and drain efficiency better than 41% - 53% at 6 dB BOP.

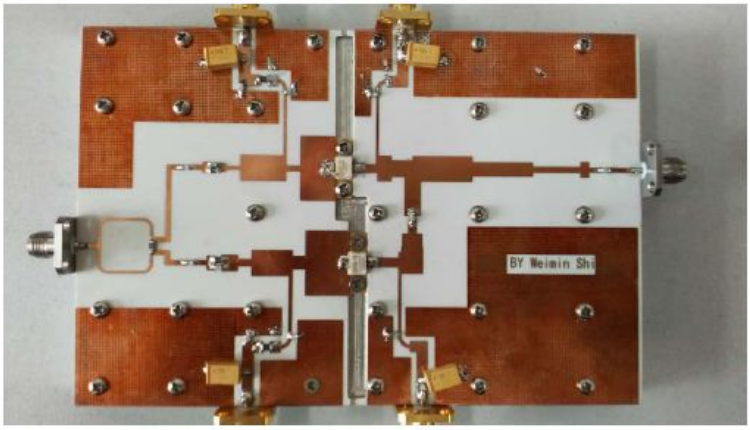


Figure 6 Photograph of the Fabricated PA [6]

D. Generalized Theory and Design Methodology of Wideband Doherty Amplifiers Applied to the Realization of an Octave-Bandwidth Prototype

Ramzi el at. [6] have worked to improve the bandwidth of the DPA by improving the combing network. This network insures the correct impedances at different power level ranges. General equations that describe the ratio between the current of the main transistor and the current of the peaking transistor are formulated. The best biasing conditions for each transistor are also identified. The following are the steps of the design as summarized by the author:

1. Firstly, find the Back-Off parameter(α). This parameter is related to the active load modulation of the peaking transistor, and it helps in controlling the dynamic power range.
2. Define the characteristic impedance of the quarter wave transmission lines of the output combiner.
3. Once the combiner is designed, this will lead to find the enhanced current factor that achieved the optimal load modulation behavior with respect to frequency.

4. The factor obtained in the previous step specifies the type of power splitter used at the input of the DPA.
5. The voltages and current profiles are obtained by the appropriate equations. Then the DC drain bias of the carrier (main) and the peaking (auxiliary) transistors are set.

Based on the steps above the final design is shown in Fig 7. The bandwidth of this design is 600 MHz (0.55-1.1 GHz), and the drain efficiency of 40% to 56% was obtained at 6 dB BOP and peak power respectively.

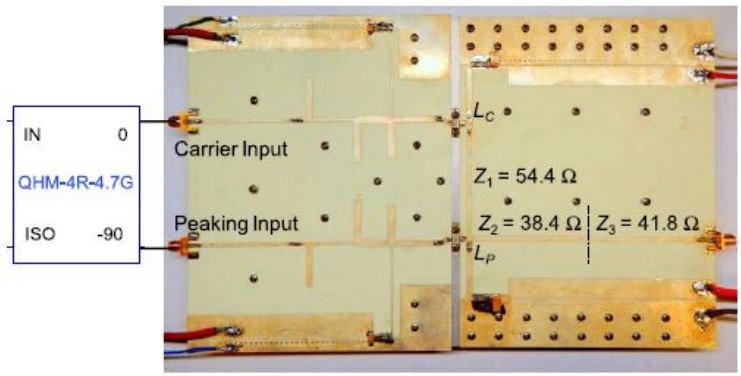


Figure 7 Photograph of the fabricated PA [7].

E. A 1.8–3.8-GHz Power Amplifier With 40% Efficiency at 8-dB Power Back-Off

SAAD et al. [4] started from the traditional Doherty power amplifier to present a new design called distributed efficient power amplifier (DEPA). The main function of this design is to overcome the limitations of the DPA.

The following figures show the topology of the DEPA and the equivalent schematics of the design in different power regions [4]

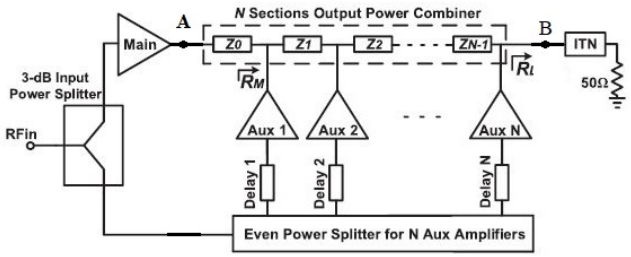


Figure 8 Topology of the DEPA PA architecture

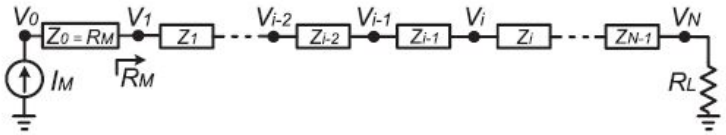


Figure 9 Equivalent schematic of the DEPA in a low-power region

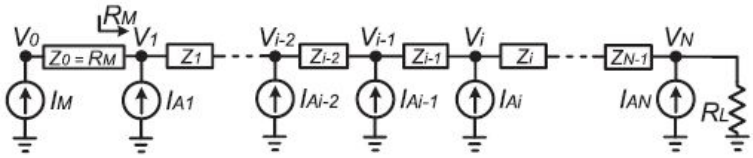


Figure 10 Equivalent schematic of the DEPA in the high-power region

The proposed topology for the DEPA is the same as that for DPA except that the auxiliary transistor is replaced by N auxiliary transistors connected to the combiner network in different points. The combiner network consists N quarter-wave transmission lines of decreasing impedances.

The principle of the DEPA is to eliminate the main reasons that produce the limitation in the bandwidth at the BOP. The N auxiliary transistors give a high degree of freedom in the design, since they turn on at the same time and connecting to the combiner network in such a way that all auxiliaries output are in phase with the main transistor. This means that the total output power is the sum of the whole transistors. Accordingly, multi sections of the combiner network will extend the bandwidth of the

PA at the BOP. The number of the combiner section depends on the bandwidth of the PA and the level of the ripples inside the operating frequency. As the number of the combiner sections is increased the ripples and the bandwidth of the PA are increased. Fig 11 depicts the photograph of the fabricated prototype of the DEPA. The measured DEPA exhibits a maximum output power of 45.4 ± 1.1 dBm and a drain efficiency of 41%–51% at 8-dB BOP across the 1.8–3.8-GHz bandwidth [4].

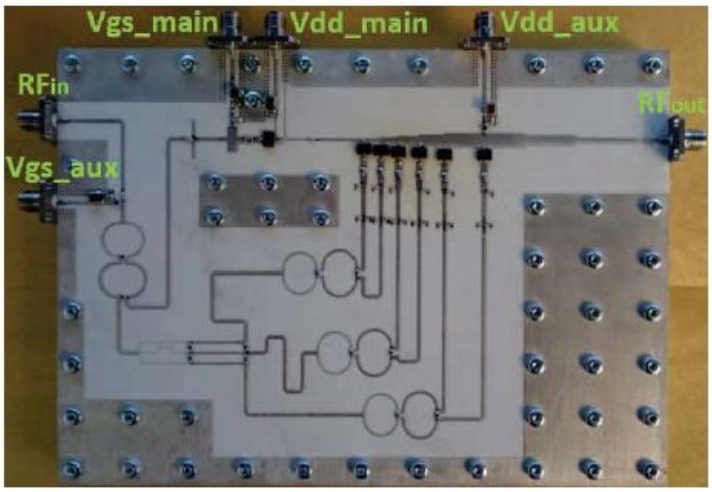


Figure 11 Photograph of the fabricated prototype of DEPA [3]

CHAPTER III

WIDEBAND POWER AMPLIFIER DESIGN, AND SIMULATIONS

A. Purpose of study:

Modern communication systems need high data bit rate. This will increase the operating frequency bandwidth and the peak to average power ratio PAPR. Hence, a new technique for power amplifier design must be used to satisfy this specifications.

The target of this study is to design a PA with a high bandwidth and a good efficiency based on the DEPA design. First, we are going to verify the results of the original version of the DEPA design by the ADS simulator. The design is then fabricated and measured to find out the matching between the simulation and measurement results. The later stage is to modify the design to get a better drain efficiency especially at the BOP level.

B. DEPA Design Methodology:

In this section, we will introduce the topology of the DEPA, then we will design and simulate all needed parts which are used in the DEPA structure. Finally, we will assemble the overall design to compare the final results with the original one.

C. Distributed Efficient Power Amplifier (DEPA) Topology:

The DEPA design concept, which is based on a multi-stage DPA architecture, is illustrated in Fig 8. The designed architecture consists of:

1. An equal power splitter block at the input
2. main transistor biased in Class-AB
3. N auxiliary transistors biased in Class-C
4. N-1 sections combiner network,
5. An output transformer network to match the output design to 50Ω load.

Unlike multi-stage DPAs, the auxiliary transistors in the DEPA design operate at the same input level. This has the advantage of removing the intermediate points between the BOP level and the saturation level. Accordingly, the load modulation effect of the combiner network is completely eliminated.

For the main transistor and the six auxiliaries, 6W Ga-HEMT deviceCGHV1F006S is used. The drain voltage is 40V, the breakdown voltage is 100V, a pinch off voltage is -3V, a knee voltage is 7V, and the saturation current is approximately 1A. The design specifications are 6W average power, 8 dB BOP, and 2 GHz bandwidth (1.8GHz – 3.8 GHz).

At the BOP level, the main transistor is matched to an optimum impedance R_{opt} to ensure a high output power and high efficiency. The multi-section combiner is used to provide a constant impedance at the output of the main transistor over the whole operating frequencies; this will extend the bandwidth of the PA. Similarly, at each junction, the auxiliaries have their optimum impedance matched to the admittance difference between the transmission line sections of the combiner. Moreover, the output waves must arrive in-phase at all junctions of the combiner network. Therefore, delay lines at the auxiliary inputs must be implemented to synchronize the timing of different signals.

a. Equal Split and Delay Lines

An equal power split is used at the input stage to divide the input power equally between the main branch and the 6 auxiliary transistors. This block mainly consists of a single 3-way even splitter. Each corresponding output is then cascaded to a wideband two-stage Wilkinson power divider in order to feed the 6 auxiliaries. Various delay lines are designed at different locations within the overall PA architecture in order to ensure that the output power is added constructively at the various junctions of the designed output combiner network.

b. Output Combiner

The output combiner network is designed to provide constant transformation between the load impedance (Point B in Fig 8) and the optimum impedance (point A in Fig 8). The combiner network consists of six equally stepped impedance sections. The load impedance is computed at the peak output power (39 dBm) as follows:

$$R_L = \frac{(V_{dd} - V_{Knee})^2}{2 \times P_{out}} = 17.5\Omega \qquad (7)$$

While the optimum load impedance is calculated at the 8 dB BOP:

$$R_{opt} = R_L \times 10^{(\frac{BOP}{10})} = 17.5 \times 10^{(\frac{8}{10})} \qquad (8)$$

$$\approx 110\Omega$$

Finally, the load impedance $R_L = 17.5\Omega$ is matched to 50Ω by using a three-section Chebyshev impedance transformer.

1. Non-Linear Model verification:

Since the non-linear model of the transistor is the bedrock of the design, we must insure that the behavior of the model is the same as the physical transistor. To do that, we have to compare the results of the model with the S-parameters of the design that

provided by the manufacturer. Fig 12 shows the schematic used to identify the RF modeling of the transistor.

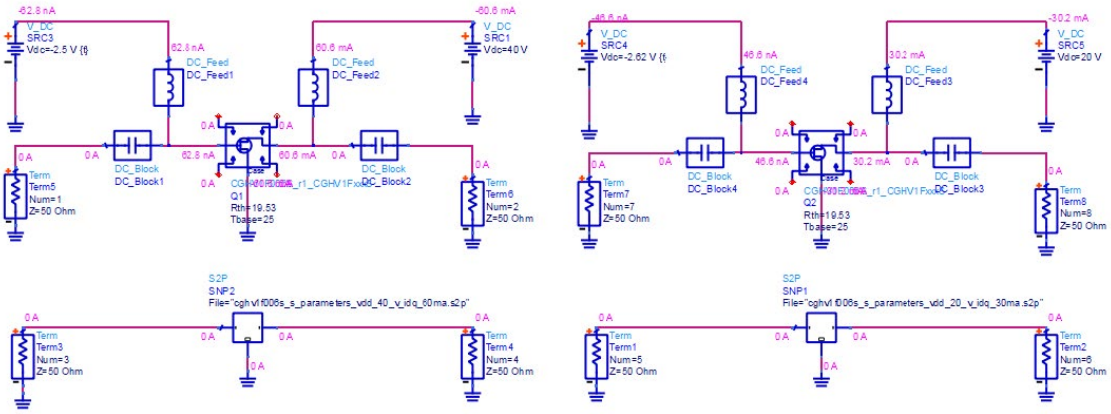


Figure 12 S-Parameters check schematics

The transistor used in this design is CGHV1F006S [4]. This device has two S-parameter results with two different biasing condition: V_{DD} = 40V with I_{QS} = 60 mA, and V_{DD} = 20V with I_{QS}=30 mA. By applying the same biasing conditions to the simulation of the non-linear model, we get the following results which are shown in Fig 13 and Fig 14.

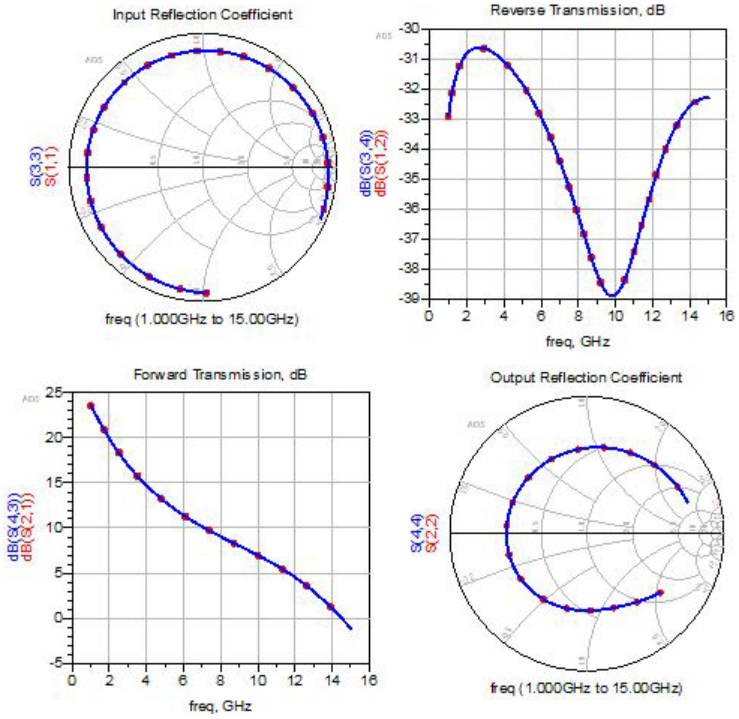


Figure 13 Comparison between the S-parameter and the non-linear model VDD = 40V, IQS = 60mA

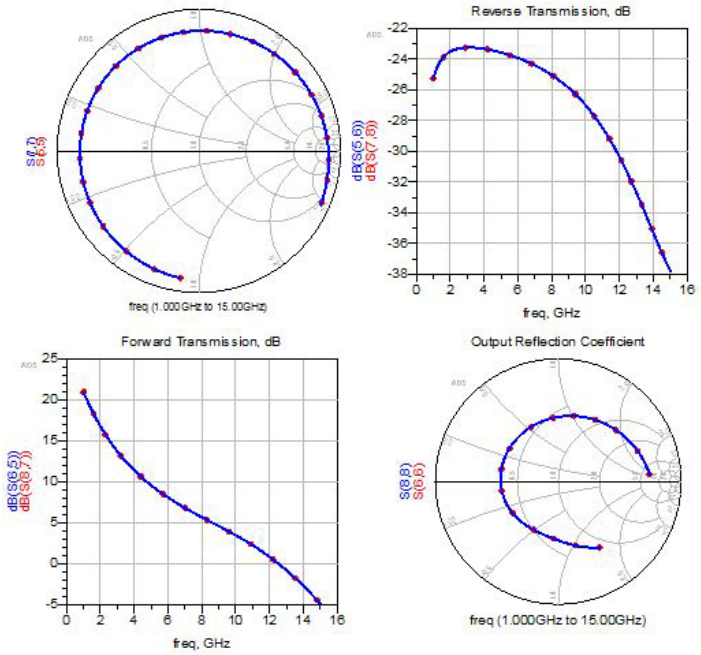


Figure 14 Comparison between the S-parameter and the non-linear model VDD = 20V, IQS = 30mA

I-V curve is another method to show the results. Fig 15 shows the schematic and the output results. It is clear that the non-linear model matched the actual transistor, and hence we are able to continue the design.

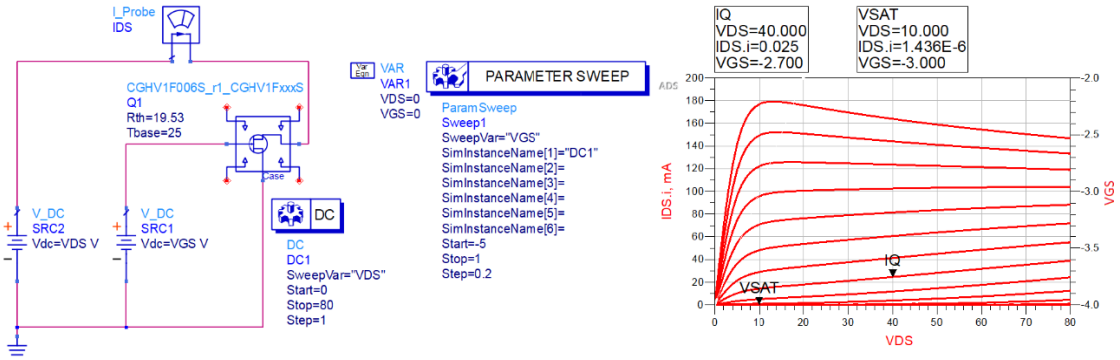


Figure 15 I-V curve method

2. *RF Stability:*

Stability is a mandatory step in any amplifier design since many transistors are conditionally stable. This can be done by validating the value of the stability factor K which must be greater than 1 in order to have a stable design. K is totally dependent on the S-parameters of the transistor, and is calculated as follows:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{9}$$

Where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{10}$$

If the transistor is potentially unstable, many techniques could be applied to the design to overcome this instability. The most common one is to add a resistor parallel to a

capacitor, and both are in series with the gate of the MOSFET as shown in Fig 16.

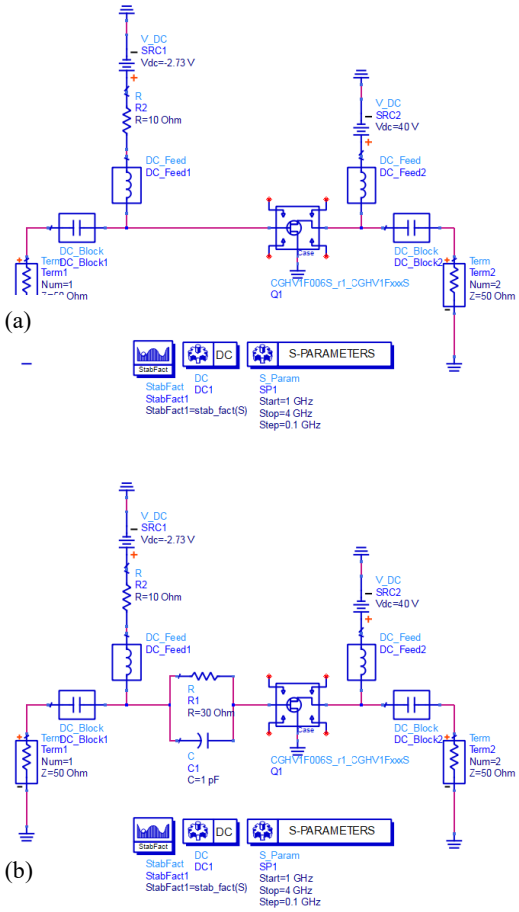


Figure 16 Schematic of the stability factor calculation (a) without stability circuit, (b) with stability circuit

The value of the stability factor before and after the stability circuit is shown in Fig. 17. The stability circuit that consists a 30Ω resistance and a 1 pF capacitor provides a stable situation

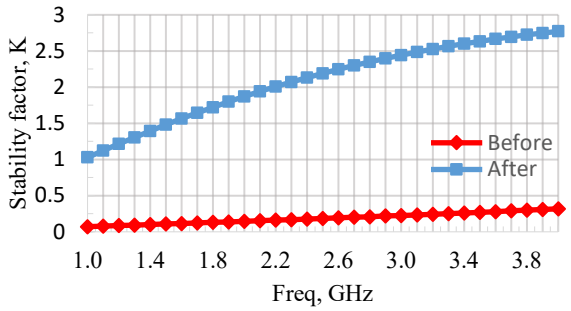


Figure 17 Stability factor value before and after using a stability circuit

3. Input Output matching circuits:

The most important issue in the PA design is the matching circuit. PA transistors always need a matching circuit to give their maximum power, so we have to design matching networks for our transistor. This is done by knowing the input and output impedances of the transistor. These impedances can be defined by using the source pull and load pull. This procedure allows us to define the compression point, gain, efficiency, and the maximum output power. CGHV1F006S transistor has a maximum output power 6 W, and the operating frequency is 100 – 15000 MHz. The load pull and source pull are shown Fig 18

At the top left side, there is a slider that selects the input power level. In this figure, the input power level is 25dBm. The red box at the bottom left side of the figure shows the value of the impedance according to a marker that exists in rectangular graph in the middle of the figure, Every time the marker called (MPdel_vs_PAE) is moved to a new position, the red box will display a new impedance. Smith chart at the top right side displays the output power and PAE contours. Each contour is related to a specific output power level and efficiency. In Fig 18, the red contours are for efficiency and the blue ones are for output power. At the left bottom side there are two graphs, one shows the gain and the compression level of the transistor and the other shows the power added efficiency.

We can clearly notice that the maximum power that could be delivered by the transistor is 37dBm (6 W) and the maximum efficiency is 60%. The compression point starts at 25 dBm with a gain of 13 dB, at the central frequency 2.8GHz of the operating band.

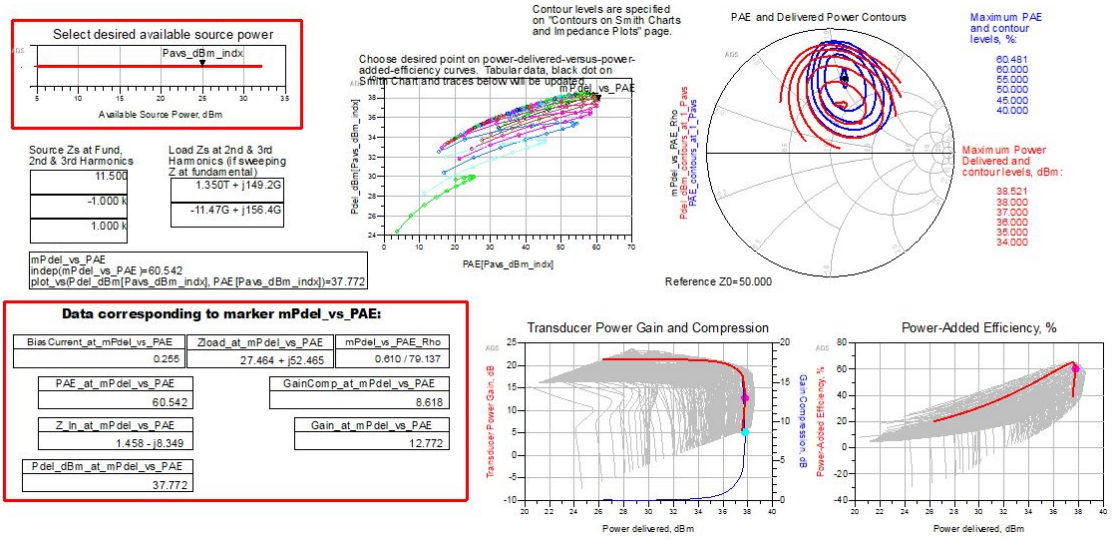


Figure 18 Load pull results, Power Added Efficiency (PAE) Vs Output Power (P_OUT)

In Fig.19, the maximum delivered output power is 38dBm. The whole results in this graphs are based on this level. One can find out the value of the output impedance of the transistor according to a minimum compression point or the high gain or the better efficiency. Now we have the output impedance of the transistor that produces the wanted output power and efficiency. The output matching network (OMN) is shown in the Fig.20. After we define the output impedance of the transistor, we have to find the input impedance. Using the source pull procedure, we are able to specify the input impedance.

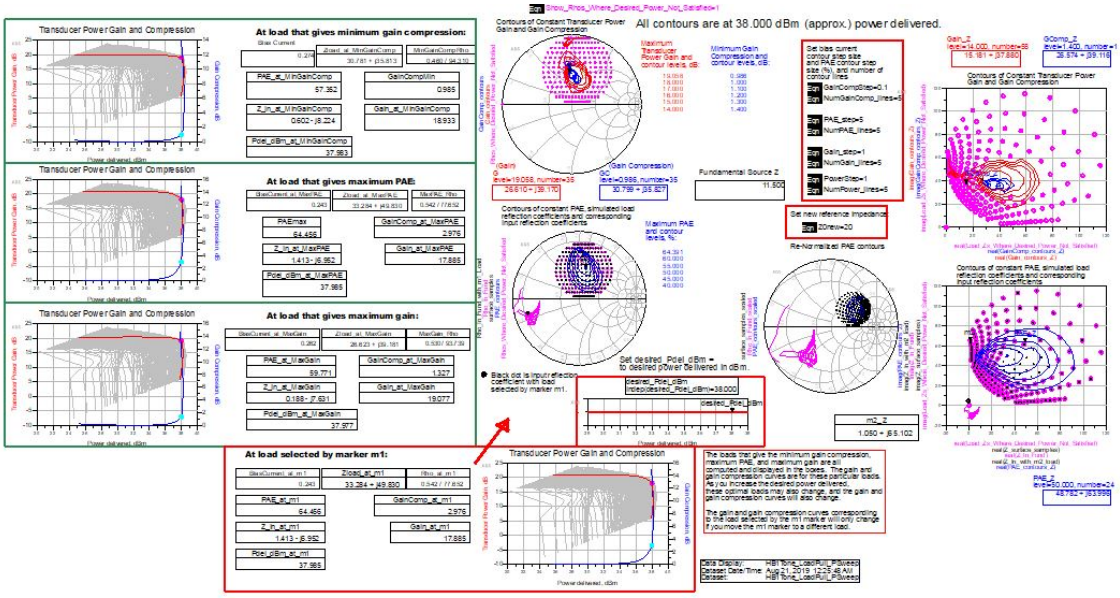


Figure 19 Load pull results are referred to the output power

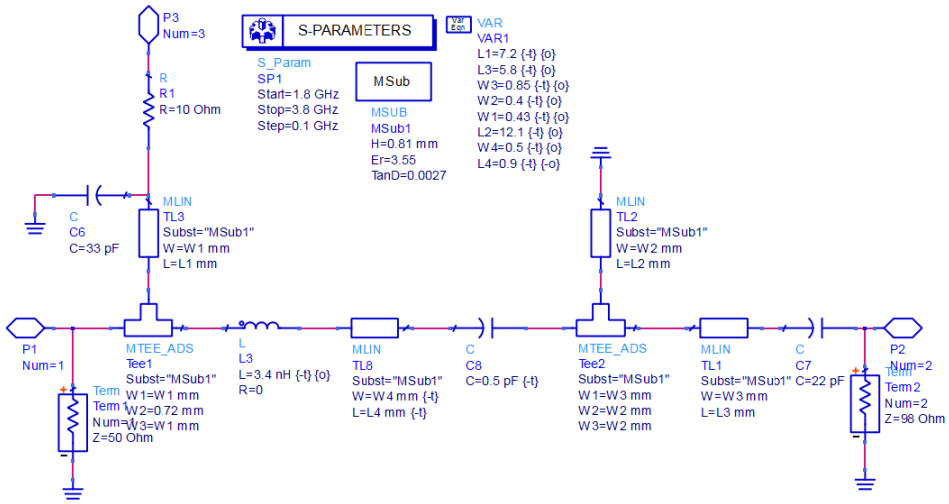


Figure 20 Output Matching Network (OMN)

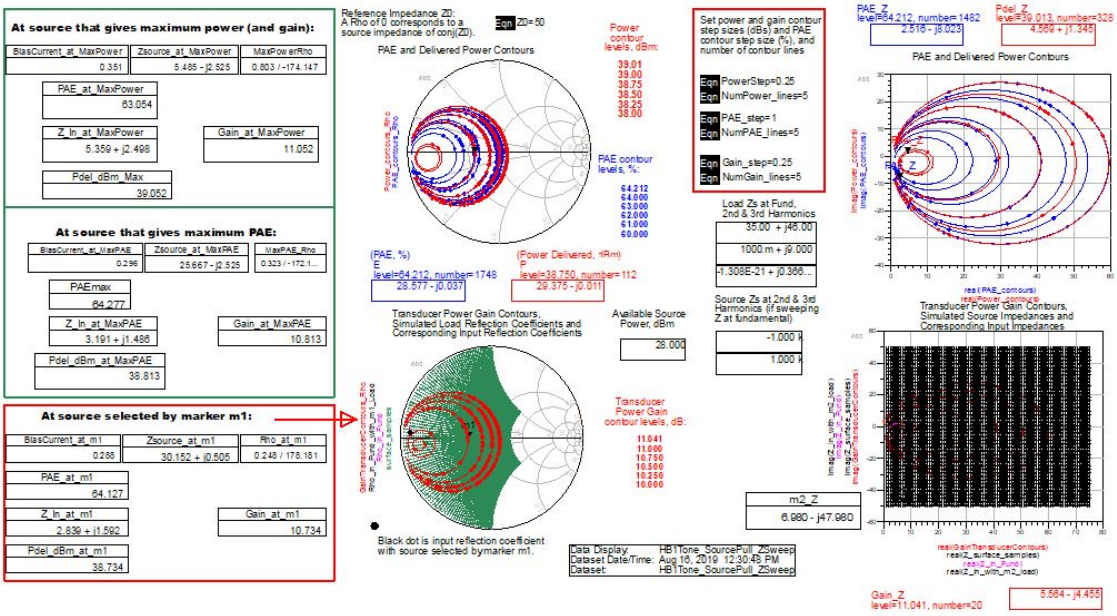


Figure 21 Source pull results PAE verses Maximum output power

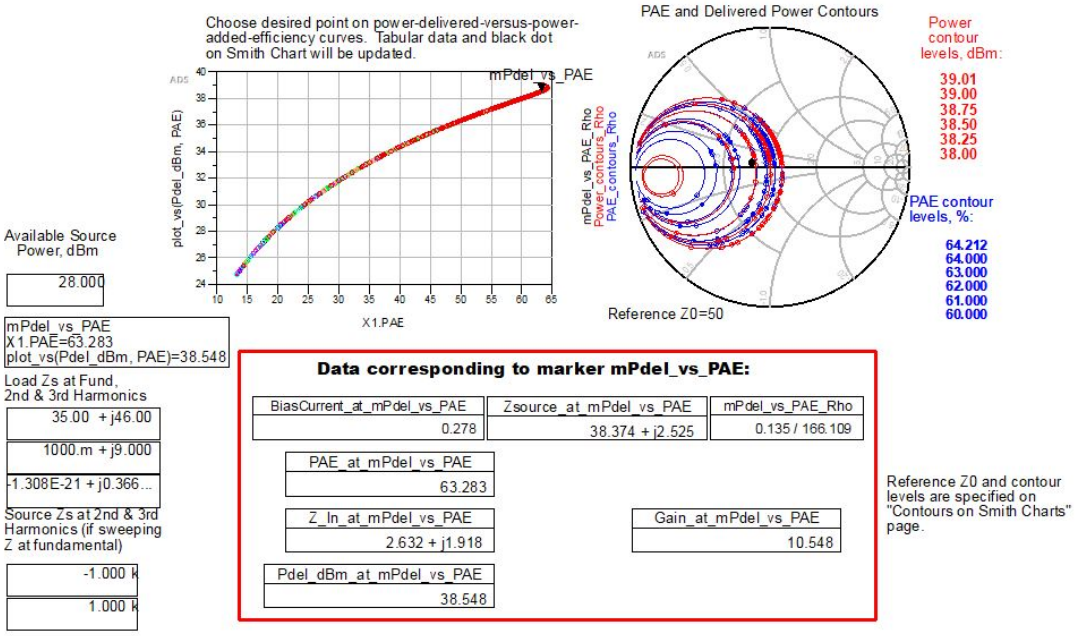


Figure 22 Source Pull contours of the PAE and maximum output power

The above figures show the results of the source pull technique where the input power used is 28dBm. Fig 22, which is a reduced version of Fig 21, focuses on the PAE and the maximum output power. As we change the position of the marker in the

rectangular graph, which it is called (MPdel_VS_PAE), the black dot in the smith chart is moved, and the input impedance according to the marker is depicted in the red box. Once we get the input impedance of the transistor at the specific frequency, we are able to make the matching circuit at the input side as shown in Fig 23.

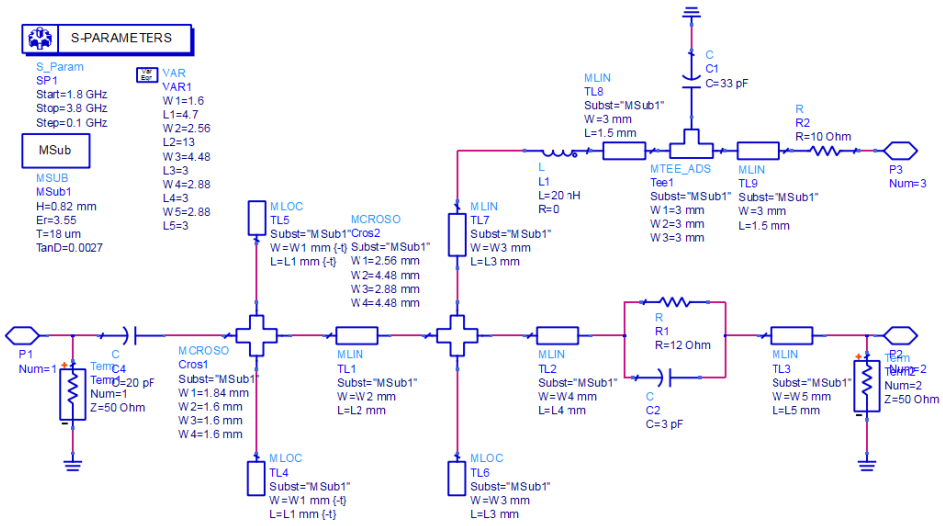


Figure 23 Input Matching Network IMN

Now we have to check the result of combining the matching circuits with the transistor. The next Fig. 24 shows the schematic of the transistor with the matching circuits.

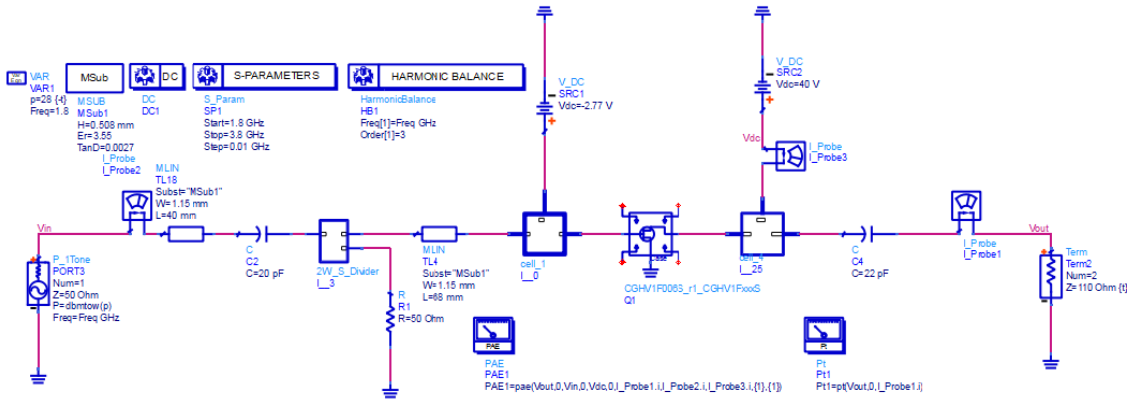


Figure 24 Schematic of a single transistor with a matching circuits at the input and the output

We can clearly observe that the results of the single transistor is perfectly matched the results of the load and source pull study. This encourages us to continue the full ODEPA design by adding the auxiliary transistors, and the power splitters. The results are illustrated in Fig 25 and Fig 26

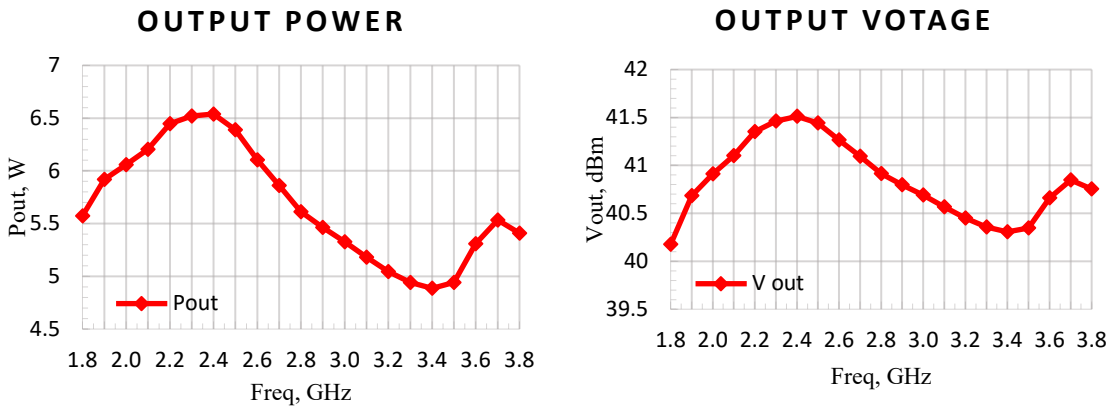


Figure 25 Output Power and Output voltage of a single transistor with IMN and OMN

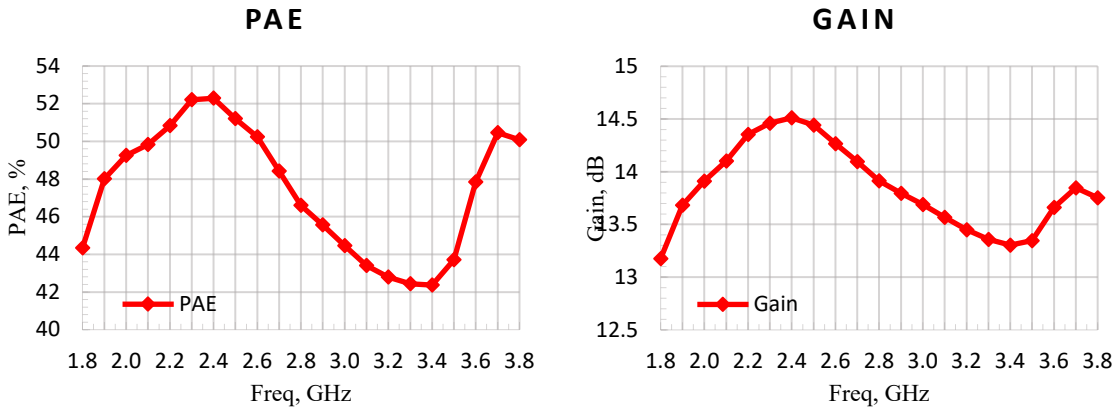


Figure 26 PAE and Gain of a single transistor with IMN and OMN

4. RF passive components:

In this design, we have two different types of power splitters, 2-Way and 3-Way splitters. In addition to ensure the wide band operation, two stage splitters are used

c. Two-Way Equal Power Splitter

Fig 27 and Fig 28 show the schematic, the layout, and the s-parameters of 2-way even splitter. The splitter has an equal insertion loss at the two output ports, and the reflection coefficients are less than (-15 dB), which is very good.

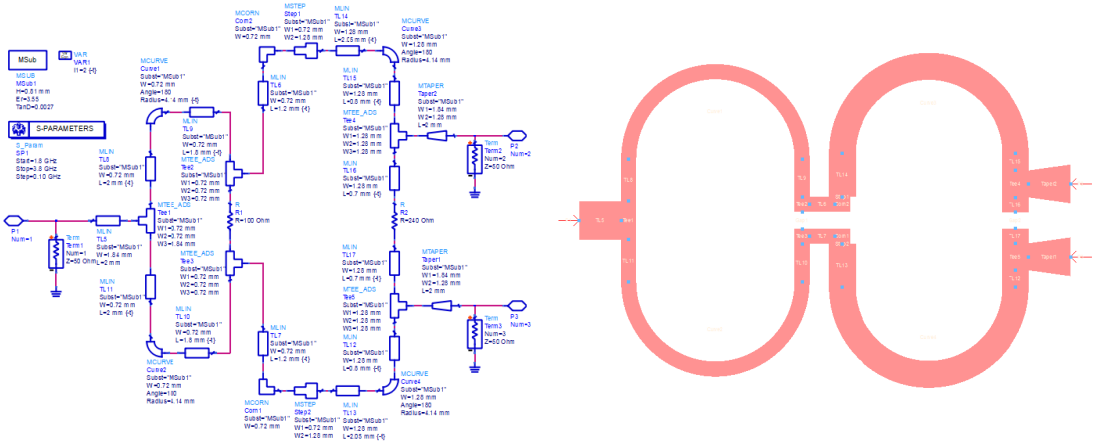


Figure 27 The schematic and Layout of the two way two stages powers splitter

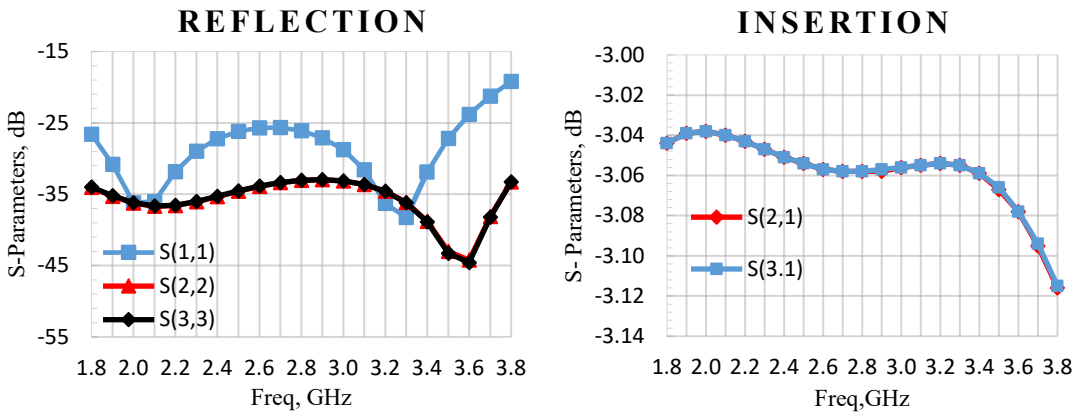


Figure 28 Reflection coefficients, and insertion loss of the two way two stages powers splitter

d. Three way Power Splitter

The results of the 3-way power splitter are very close to the theoretical one. The insertion loss at three output ports is about (-4.8 dB), and the reflection coefficients at all ports are less then (-15 dB) as shown in Fig 30

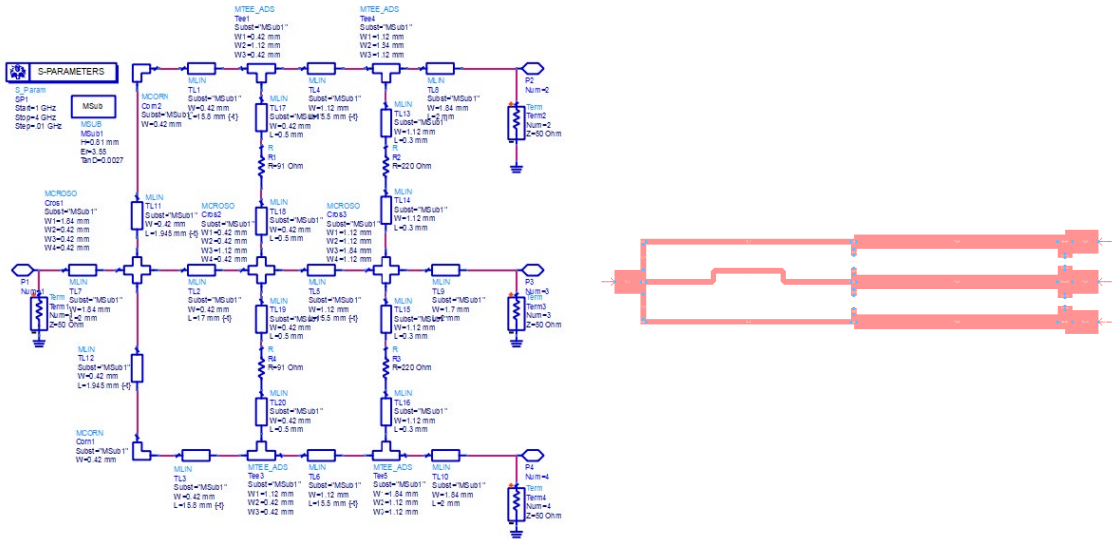


Figure 29 The schematic and Layout of the 3-Way 2- Stages power splitter

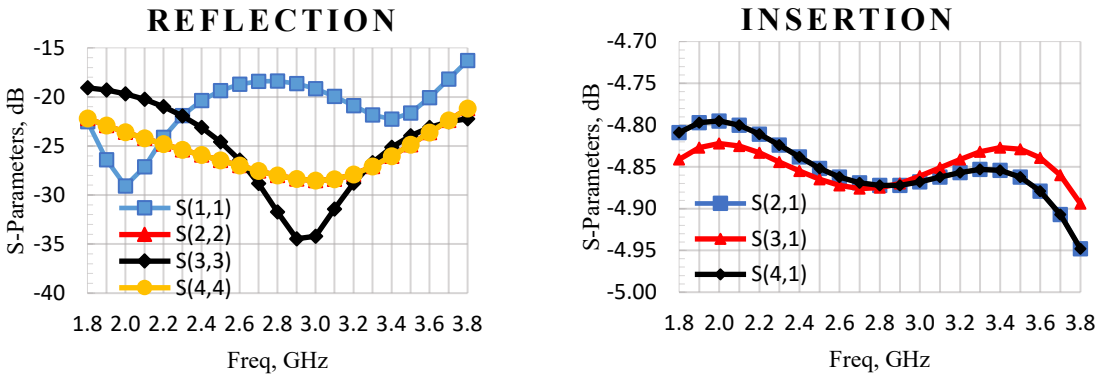


Figure 30 Reflection coefficients, and insertion loss 3-Way 2- Stages power splitter

5. Distributed Efficient Power Amplifier (DEPA) Simulations:

The final step is to simulate the complete design by connecting all parts. The passive splitters, the matching networks, the combiner network, the inverse transfer

network, and the auxiliary circuits are all put together in order to achieve a design that resembles the one depicted in [4]. The complete design of the PA helps to understand the functionality of the design which leds to improve the performance of the PA in the upcoming stages.

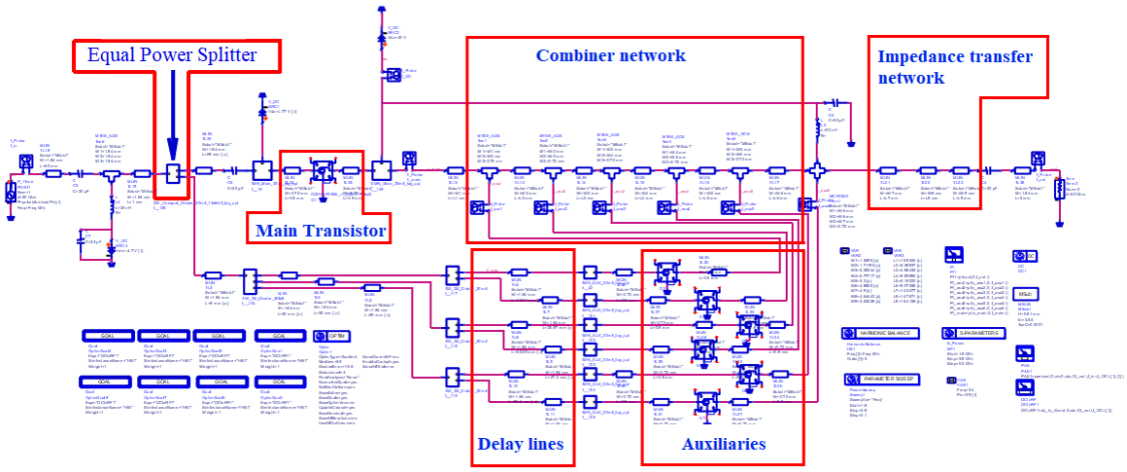


Figure 31 Schematic of the complete DEPA design

The original design is fabricated on RO4003C substrate having 20mil thickness. Whereas the available board is RO4350B with a 32mil substrate thickness. This means that if the same dimensions mentioned in the paper are used, we will not get the same results because the thicker substrate will introduce some losses to our design. Consequently we re-optimized the IMN, OMN, combiner network, and the delay lines, to overcome these losses and to get a perfect matching with the original design.

The total output power is equal to 30 W at the central frequency due to the constructive addition of power from main and auxiliary transistors. The total drain efficiency of the design across the bandwidth 1.8-3.8 GHz is 46% - 51%. Fig 32 shows that the original design has somehow better results than the optimized one at the peak power. Actually, this was expectable

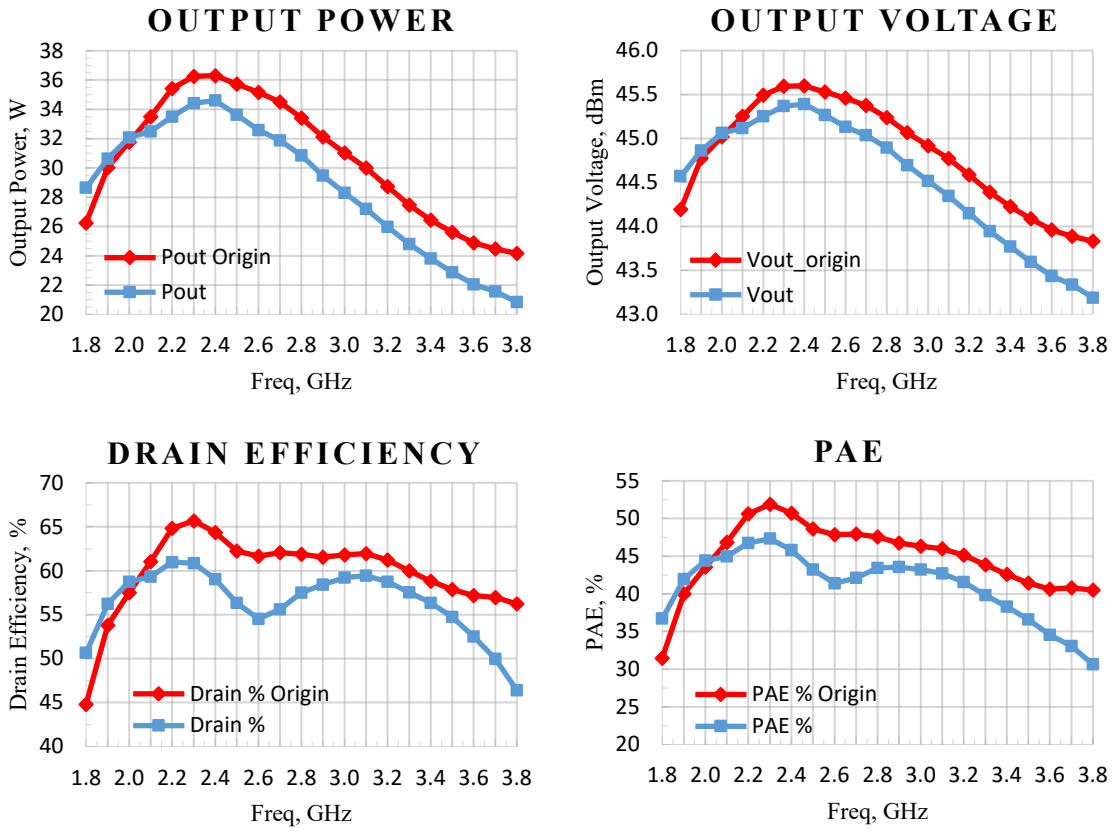


Figure 32 Output results of the complete design at peak power (Pin = 39dBm), Red line is the optimized design, blue line is the original design

Fig 33 clearly shows that the optimized design has somehow better results at 8 dB BOP level than the original one. This is very important since the main objective of this work is to get a good efficiency at the BOP level. But as a conclusion we could say that the two design have the same results, and we can go forward to fabricate the design for measurements.

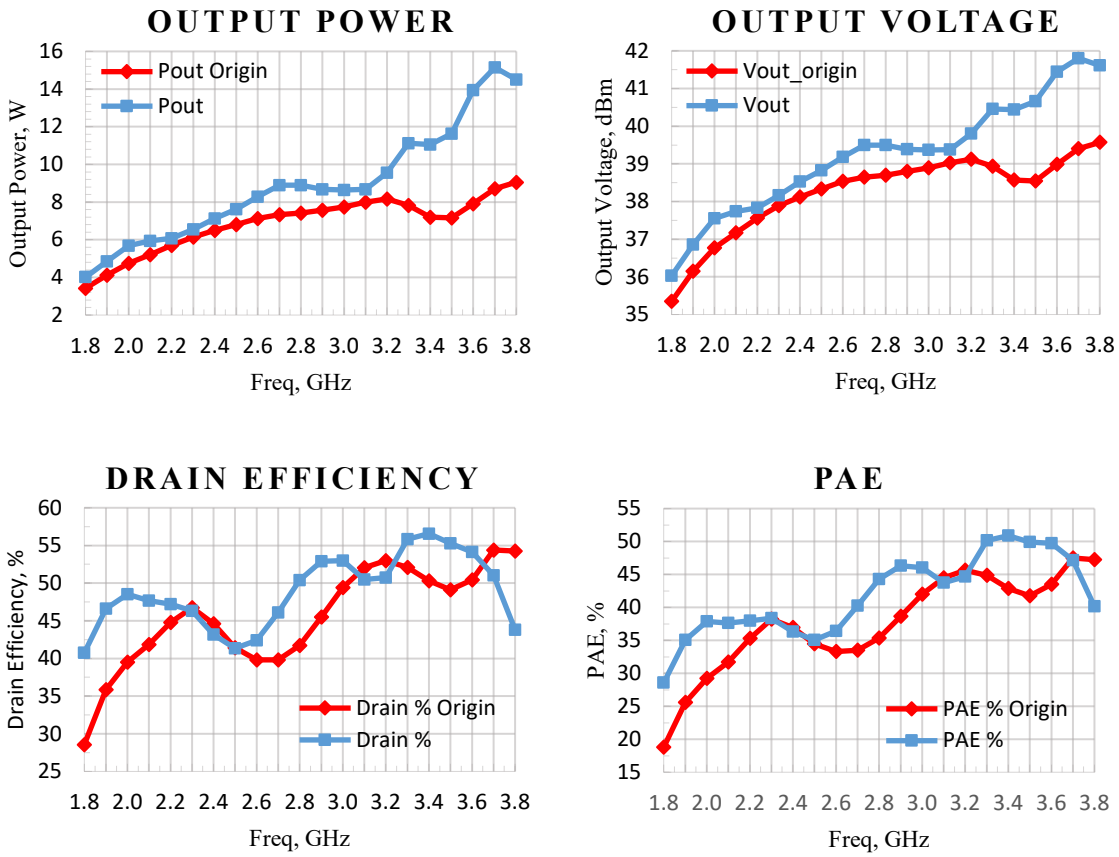


Figure 33 Output results of the complete design at 8dB BOP (Pin = 31dBm), Red line is optimized design, blue line is the original design

D. Optimized Distributed Efficient Power Amplifier (ODEPA) Simulation:

In order to improve the performance of the PA, two different methods are suggested. First method is replacing the equal power slitter by unequal power splitter at the input of the PA since we noticed, during the study, that the main transistor goes deeply in compression region. So the unequal power splitter will reduce the input power level at main branch, and hence increases the efficiency of the whole design. Second suggested method is to add matching circuits at the output of the auxiliary transistors to improve their functionality. Since the combiner network, that adds the output signals of the auxiliary transistors to the output signal of the main in a constructive way, must also

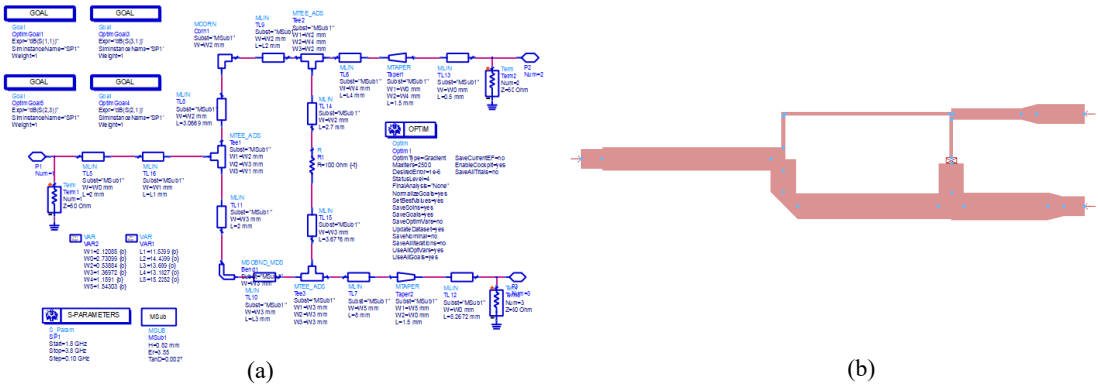
compensate the output impedance parasitic of the auxiliaries. But since we are designing a wideband PA, it will be difficult to insure that.

1. First Method (Unequal Power Splitter)

Three different power splitters are considered for implementation in the overall PA structure. Namely, 2-4 dB, 1.5-4.5 dB, and 1-5 dB are investigated.

a. 2-4 dB Unequal Power Splitter:

Fig 34 and Fig 35 depict the schematic, the layout, the reflection coefficients and the insertion loss of the 2-4 dB power splitter. The results show that reflection coefficient at port 2 is not totally less than (-15dB), but this is not an issue since the feeding port (1) has a good reflection coefficient. Also the insertion loss over the whole band is approximately equal to what we expected. That is, around -2.2 dB for port 2, while port 3 has an insertion loss around -4.2 dB



(a) (b)

Figure 34 2-Way 2-4 unequal power splitter (a) schematic, (b) Layout

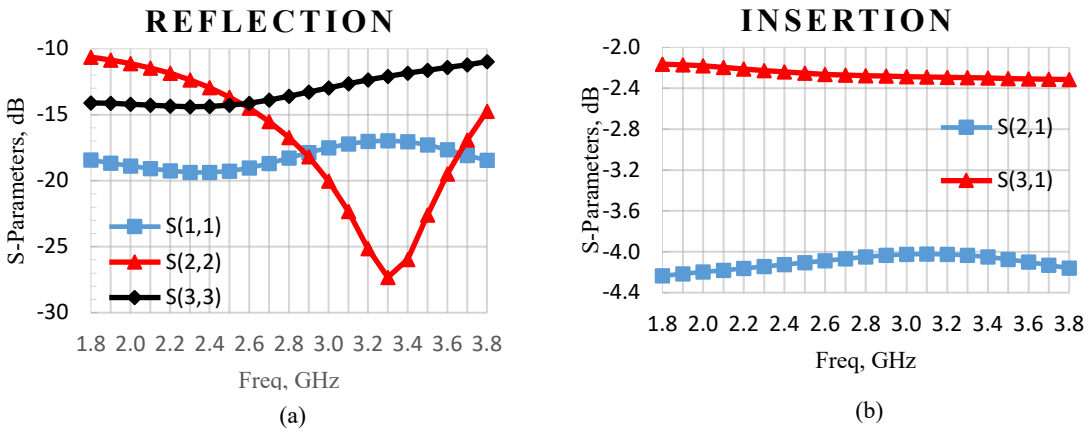


Figure 35 2-Way 2-4 unequal power splitter (a) Reflection coefficients and (b) insertion loss

b. 1.5-4.5 dB Unequal Power Splitter:

Fig 36 shows the schematic and the layout of the second alternative 1.5-4.5 dB power splitter, while Fig 37 shows the reflection coefficients and the insertion loss. It is clear that as the splitting ratio increases between the two ports, it becomes difficult to achieve the target output levels. The insertion loss at port 2 and 3 are - 5.2 dB and -1.8 dB respectively, which it is slightly shifted from the expected level. Also you can notice that the reflection coefficients at the output ports 2 and 3 are not as good as we hope. But we still have a good input reflection coefficient at the input port $S_{1,1}$.

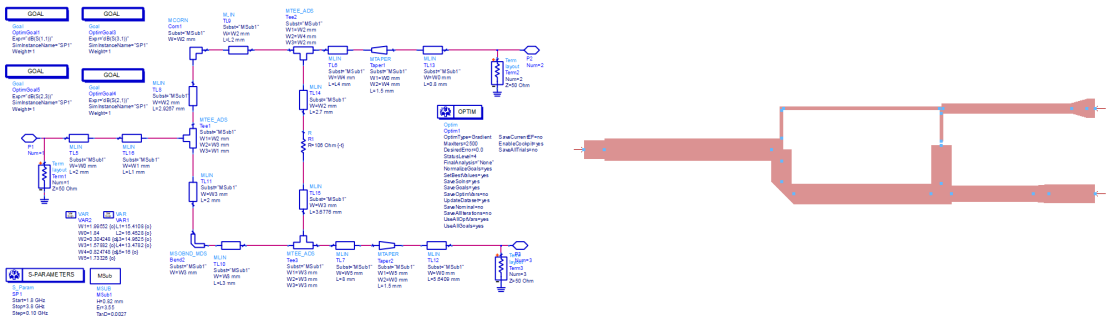


Figure 36 2-Way 1.5-4.5 unequal power splitter (a) schematic, (b) Layout

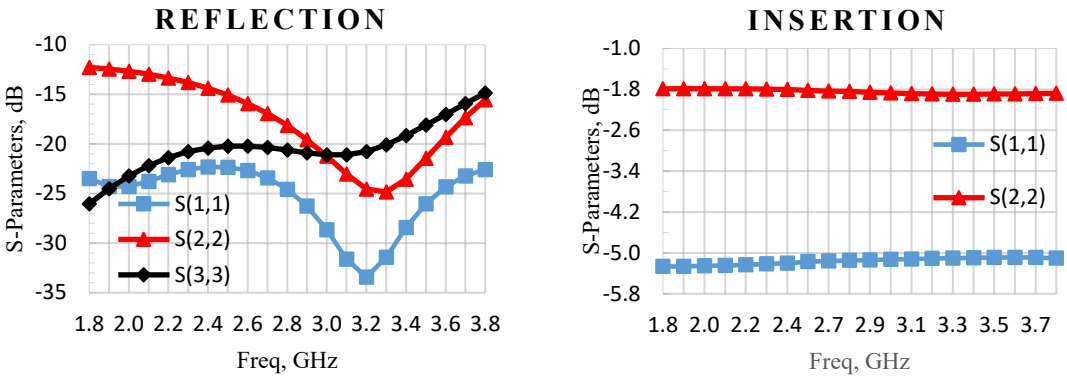


Figure 37 2-Way 1.5-4.5 unequal power splitter (a) Reflection coefficients and (b) insertion loss

c. 1-5 dB unequal Power splitter

The last alternative is the 1-5 power splitter. Again the results are not matched to the requirements. The insertion loss at port 2 and 3 are approximately (-6.8 dB and -1.3 dB) respectively. While the reflection coefficient at the input port is less than -15 dB, as, as shown in Fig 39

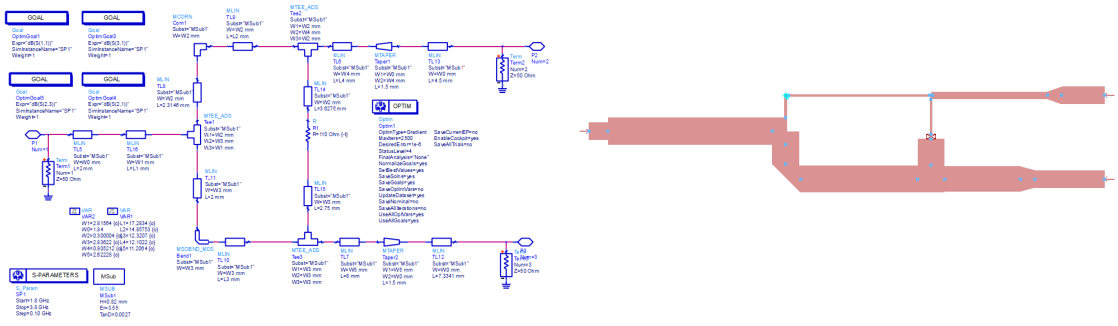


Figure 38 2-Way 1-5 unequal power splitter (a) schematic, (b) Layout

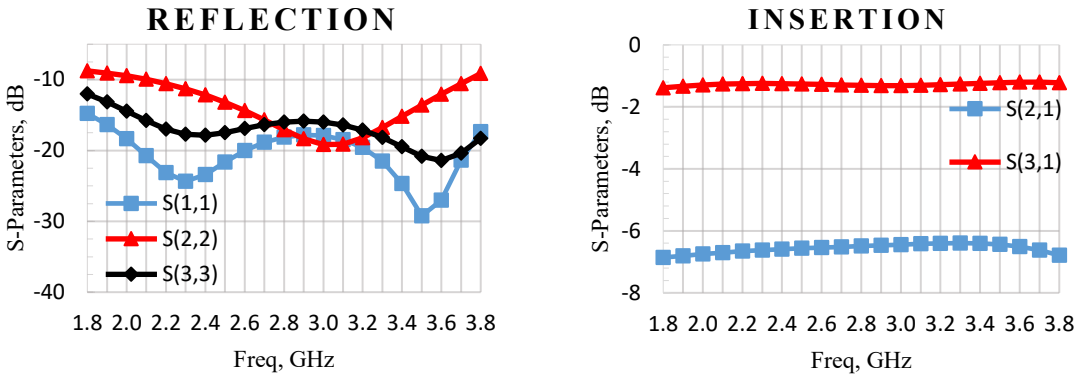


Figure 39 2-Way 1-5 unequal power splitter (a) Reflection coefficients and (b) insertion loss

2. *Optimized Distributed Efficient Power amplifier (ODEPA) Simulation*

The proposed design concept, which is based on a multi-stage DPA architecture, is illustrated in Fig 40. Three Unequal power splits are applied at the input stage of the PA in order to improve the performance of the DEPA. Since the signal levels at the input of main and auxiliary transistors are changed, the whole dimensions of each component in the structure must be re-optimized. These components are the combiner network, the delay lines, input output matching networks and the transfer network. The schematic of the proposed design is depicted in Fig 41

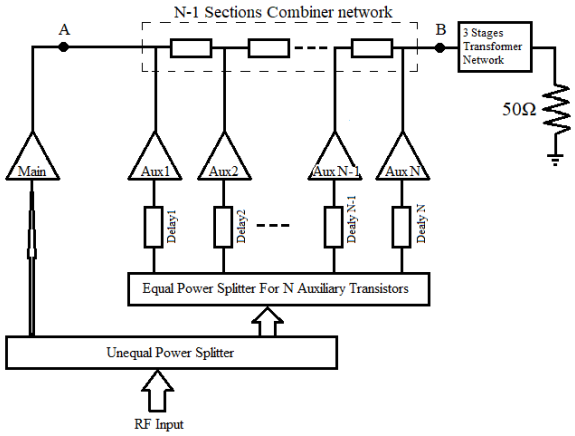


Figure 40 Proposed design concept

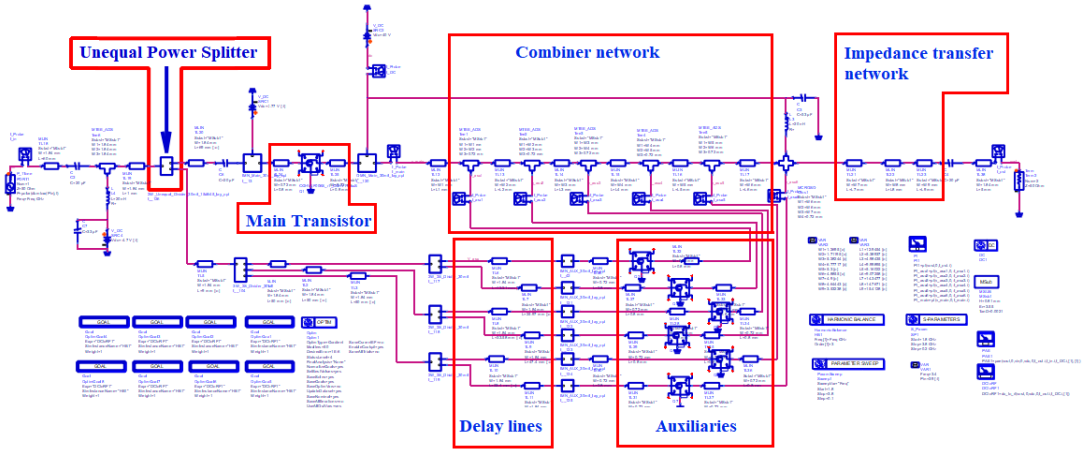


Figure 41 Schematic of the proposed design

It was empirically determined that the 1.5-4.5 dB splitter gives the best performance since the output efficiency at the 8 dB BOP is increased by 5-10 %, and the output power is also enhanced by 2-3 dBm in comparison to the case when equal power split is adopted. It is important to note that the main transistor is driven by the lower power level (i.e., -4.5 dB). Fig42 illustrates the final results.

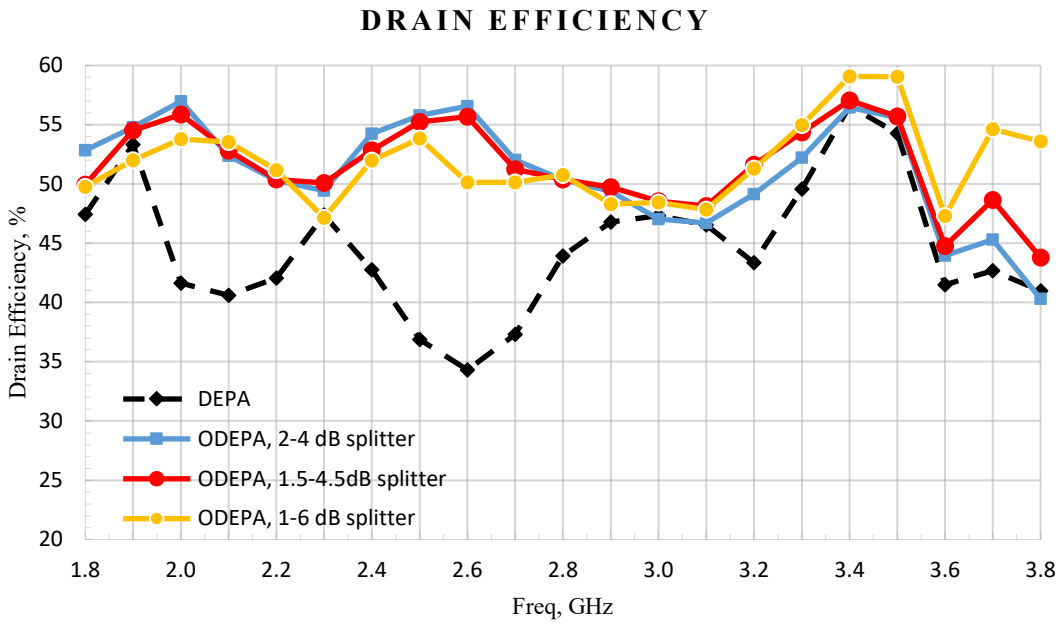


Figure 42 Drain efficiency of different power splitters at 8dB BOP level

It is clear that all different types of the unequal splitters give a better performance than the equal power splitter. This was expected since the input power level at the main branch was reduced, hence the compression level of the main transistor decreased and accordingly the drain efficiency is improved.

All simulations done so far are based on an ideal case. So after choosing the power split that gives the best performance, another step must be accomplished. For the layout to be achievable, extra components must be added to it. For example, the transistor used in this design needs small transmission lines at the input and the output. These lines allow the transistor to be soldered on the board. As depicted in Fig 43

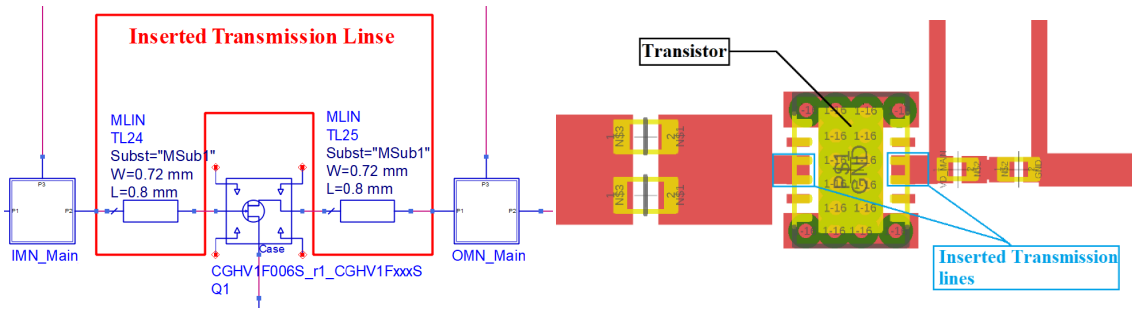


Figure 43 Inserted transmission lines, schematic and layout

To investigate the effect of the new components, another simulation is performed. Fig 44 shows the degradation of the drain efficiency at the high frequency. Hence, an optimization process must be repeated again to adjust the dimensions of the components in the design.

The final results in Fig 45 show that the drain efficiency after optimization is very close to the ideal case, and the effect of transmission lines is approximately removed, so we are ready to fabricate the proposed design for measurements.

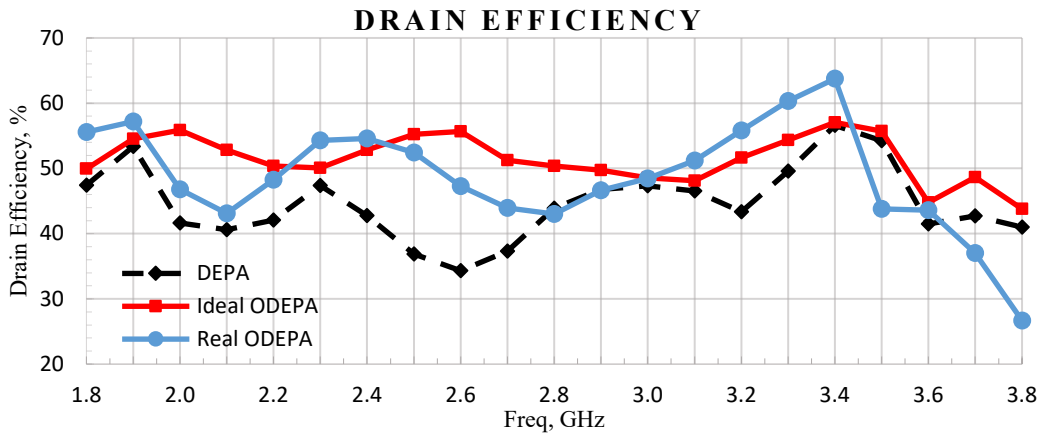


Figure 44 Effect of the transmission lines on the drain efficiency at 8 dB BOP level

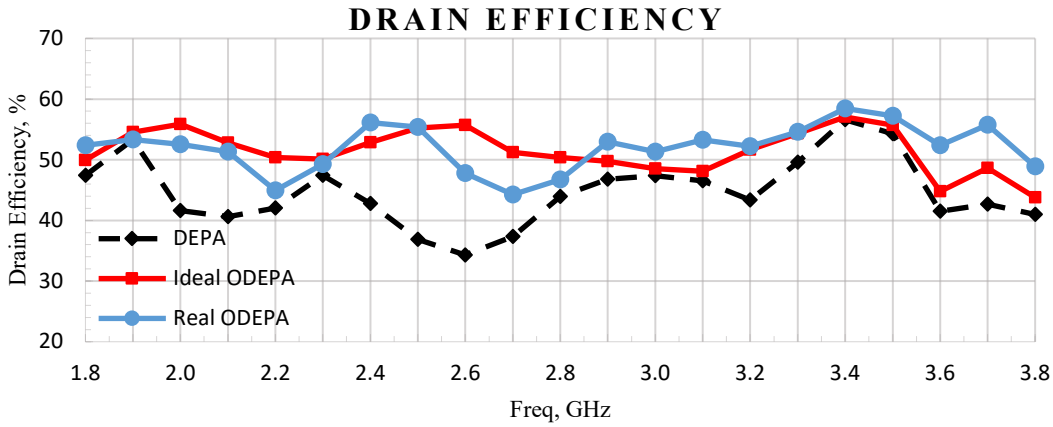


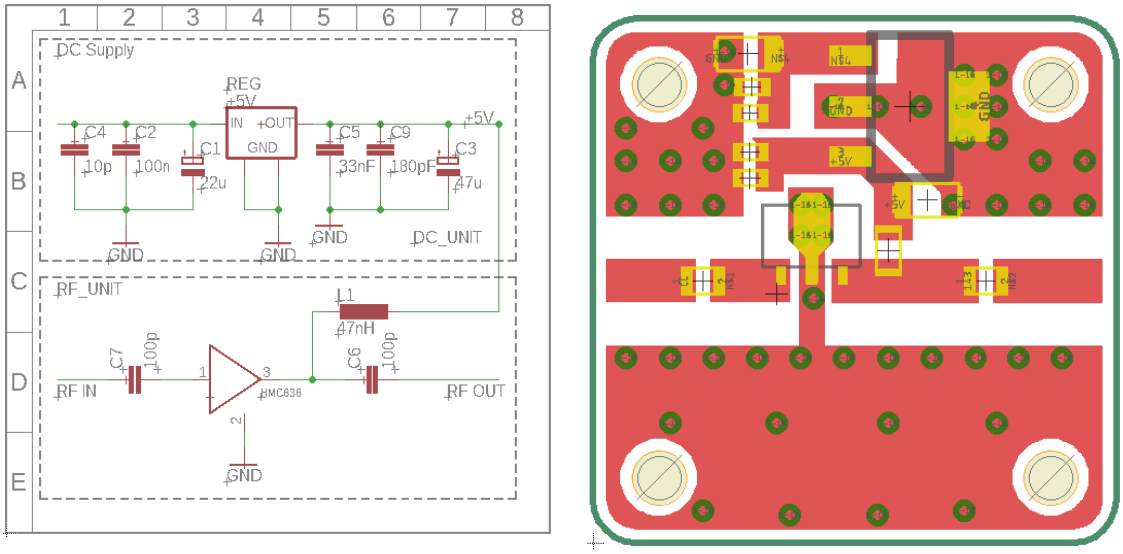
Figure 45 Drain efficiency of the final optimized design at 8 dB BOP level

E. Block Gain and Driver amplifiers:

The maximum output level of the signal generator at the LAB is about +10dBm while the peak power level of our design is about +39dBm. So we have to increase the level of the signal to be fed to the PA, otherwise the measurements would not be established. A gain block and driver amplifiers must be designed to provide the required levels.

HMC636 transistor is used for the gain block amplifier. It operates up to 4GHz with a gain of +13dB, the 1dB compression point of about +22dB at the output. Just like any transistor, the gain of the device is reduced as the operating frequency is increased. So a higher input level is required at the higher frequencies. On the otherhand, the output level of the signal generator is also decreased at higher frequencies. This will pose a limitation in the measurement procedure.

The input and output of the transistor is internally matched to 50 Ω, the



schematic and the layout of the gain block are shown in Fig. 46. FR4 with 1mm substrate thickness is used.

Figure 46 Schematic and layout of the gain block

Until now, the signal level is about +22dBm. This means that the driver amplifier must rise the signal level up to +39dBm. GHV1F006S transistor is used for the driver and the input/output impedances of the transistor are known from the previous study. Hence, input and output matching networks are designed to have a wideband driver amplifier. The transistor gives between 6 and 7W at the output, which means that the driver is able to rise the signal up to approximately +37 - +38 dBm. The

layout is fabricated on FR4 with 0.8mm substrate thickness and the schematic and the layout are shown in Fig 47.

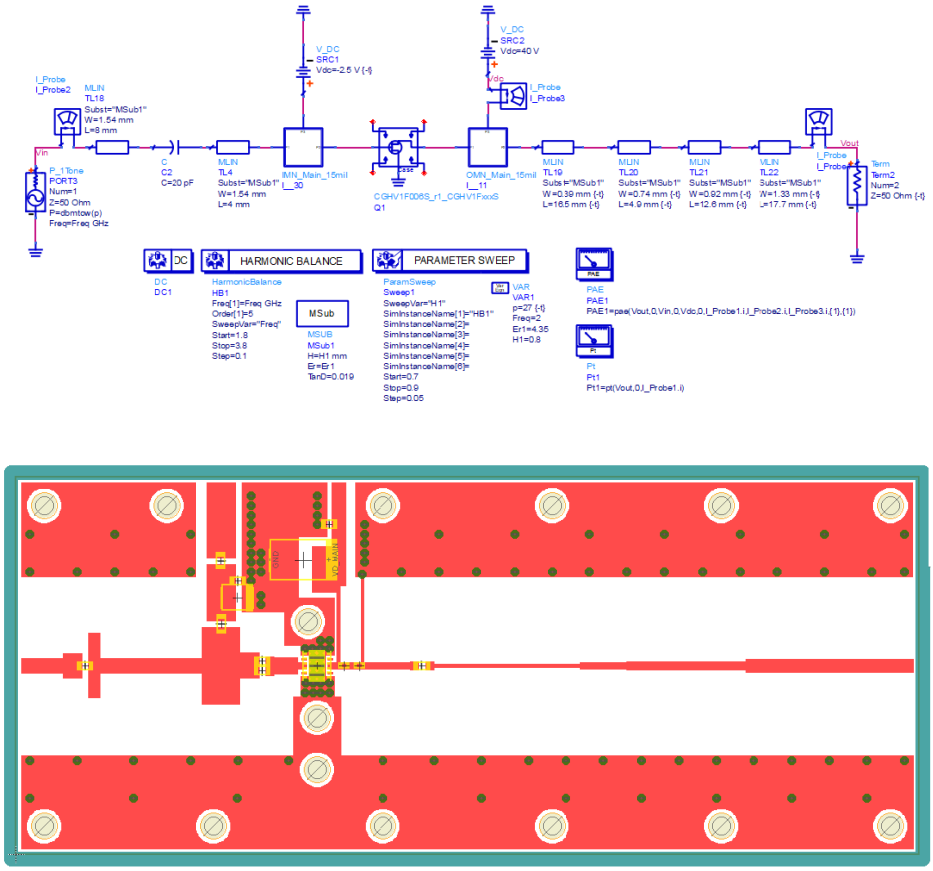


Figure 47 Schematic and Layout of the Driver

Since the FR4 does not has an accurate thickness and dielectric constant (ε_r), additional simulations are accomplished to ensure that the performance of the driver amplifier does not vary very much with the change of the FR4 board parameters. The output results showed that the driver design is robust and the output level is almost constant. The output level of the driver with respect to thickness and dielectric constant changes are depicted in Fig 48 and Fig49 respectively.

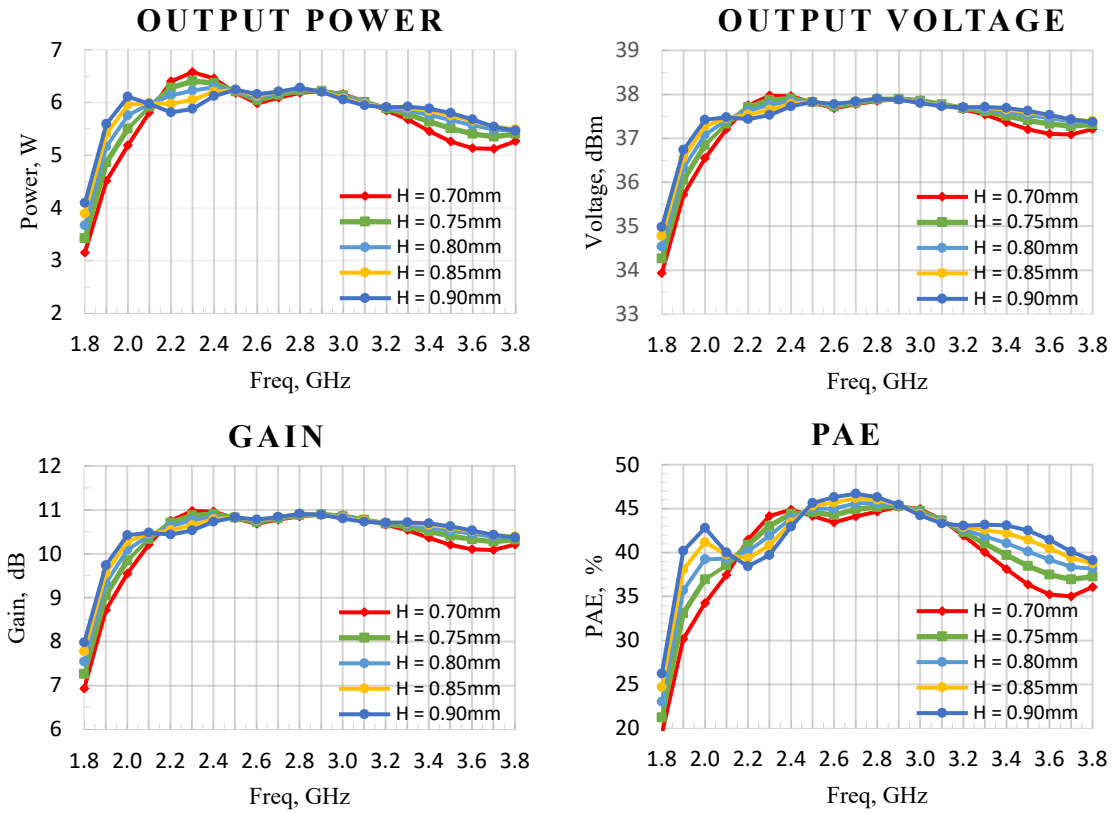


Figure 48 Driver output response with respect to different board thicknesses

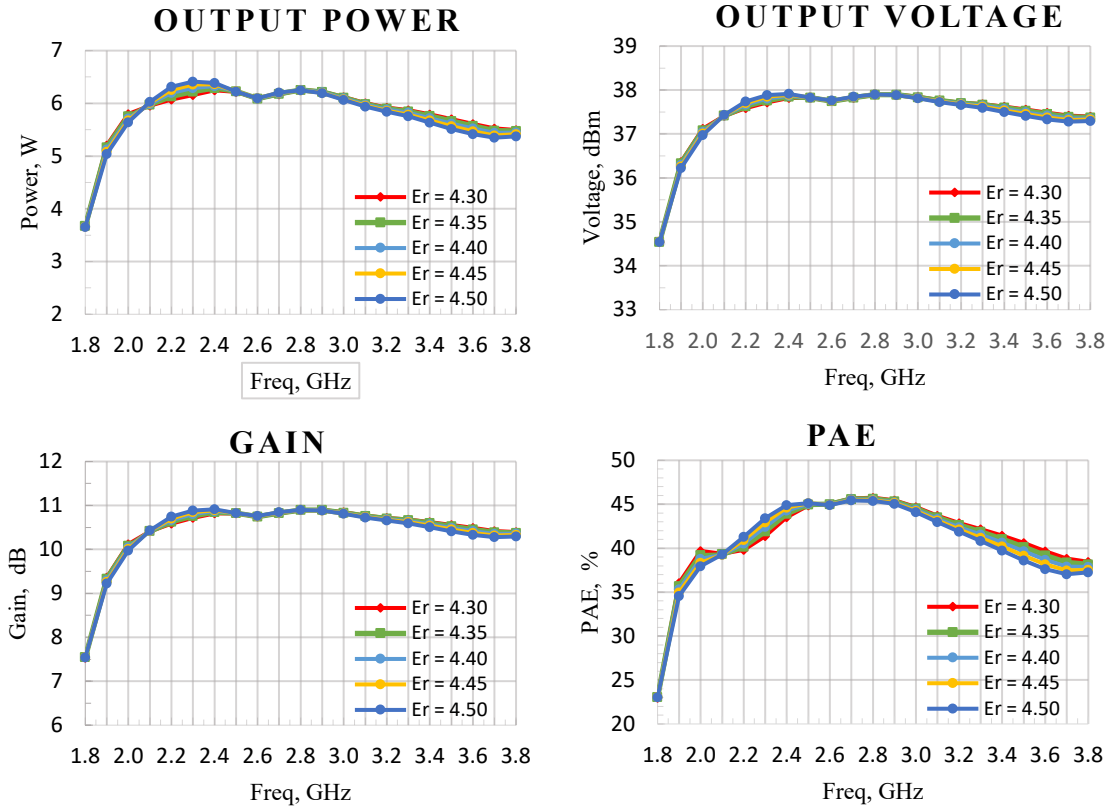


Figure 49 Driver output response with respect to different board dielectric constant

Finally, the relationship between the input power level, the output power level, the efficiency and the gain of the driver is investigated in the last simulation for a different frequency in the operating band (1.8 – 3.8 GHz). Obtained results are plotted in the Fig 50

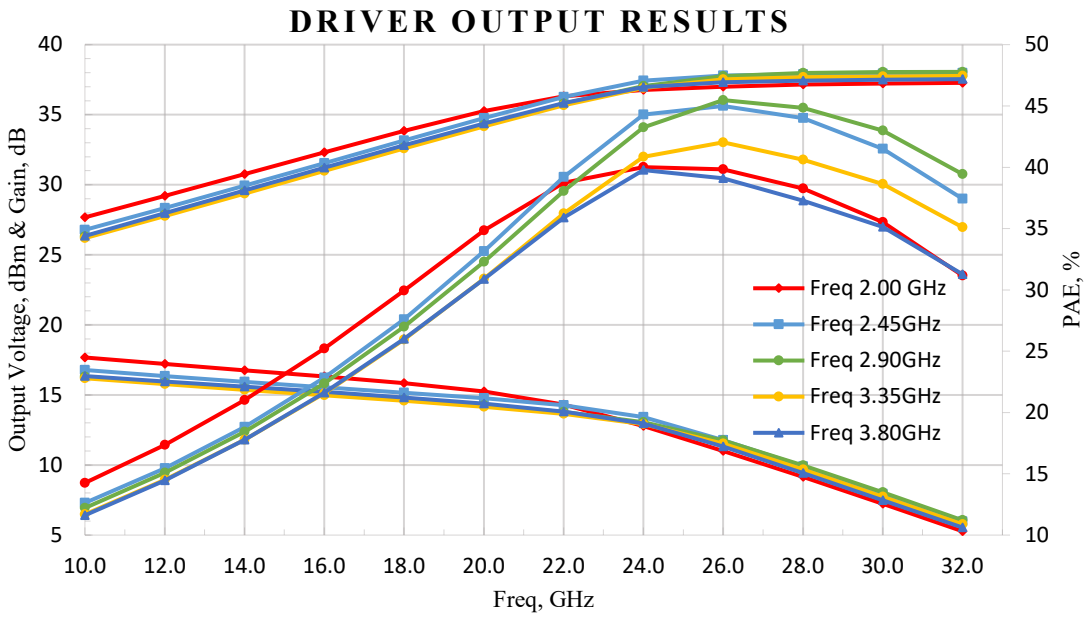


Figure 50 Output Voltage, Gain, and PAE of the driver amplifier

CHAPTER IV

IMPLEMENTATION AND EXPERIMENTAL RESULTS:

In this section the measuring requirements, the procedure, and the final results will be introduced.

A. Measuring requirements:

1. Test set component

Measuring the power amplifier needs a special test set to protect the instruments at the LAB, since the signal level of most PAs is higher than +30dBm. This level is usually the absolute rating that can break most equipment. The test set consists of an attenuator, a coupler, and a dummy load. Moreover, the components used for measurement must sustain the signal level of the device under test. Fig 51 shows the structure of the test set. The components used in this work are described below.

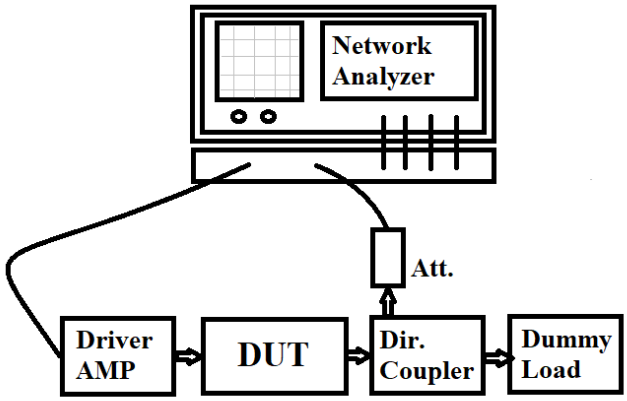


Figure 51 Structure of the test set

Table 1: Test Set Components

Component	Description	Photo
Attenuator	• Power 20W • Operating Frequency DC-6GHz, • 20dB attenuation • 50ohm • N-type connector,	
Dummy Load	• Power 50W • Operating Frequency DC-6GHz • 50ohm • N-type connector	
Directional Coupler	• Power 50W • Operating Frequency 1 - 4GHz • 50ohm • SMA connector • Coupling 10dB, Directivity MIN 20dB	

The output of the power amplifier is directly connected to the dummy load, while a part of the signal is coupled to the signal analyzer through the attenuator, so the signal level is reduced by about 30 dB.

2. 40V Power Supply:

The transistor used in this design operates at 20 and 40 V, but it is recommended to work at the higher voltage. At the LAB, there are many power supplies that can be used to provide a 40 V, but this will consume many of them to provide the DC level for the power amplifiers, since we have the driver and the proposed design amplifiers.

A booster DC-DC converter is designed to solve this problem. It has an input range of 15 to 25 V and two 40 V outputs while the output current is dependent on the

input voltage. For example, if the input voltage is 20V, the output current can be delivered is 1.2A.

LM2577 booster device is used in this power supply. The schematic, the layout and the fabricated design of the DC-DC converter are shown in Fig 52.

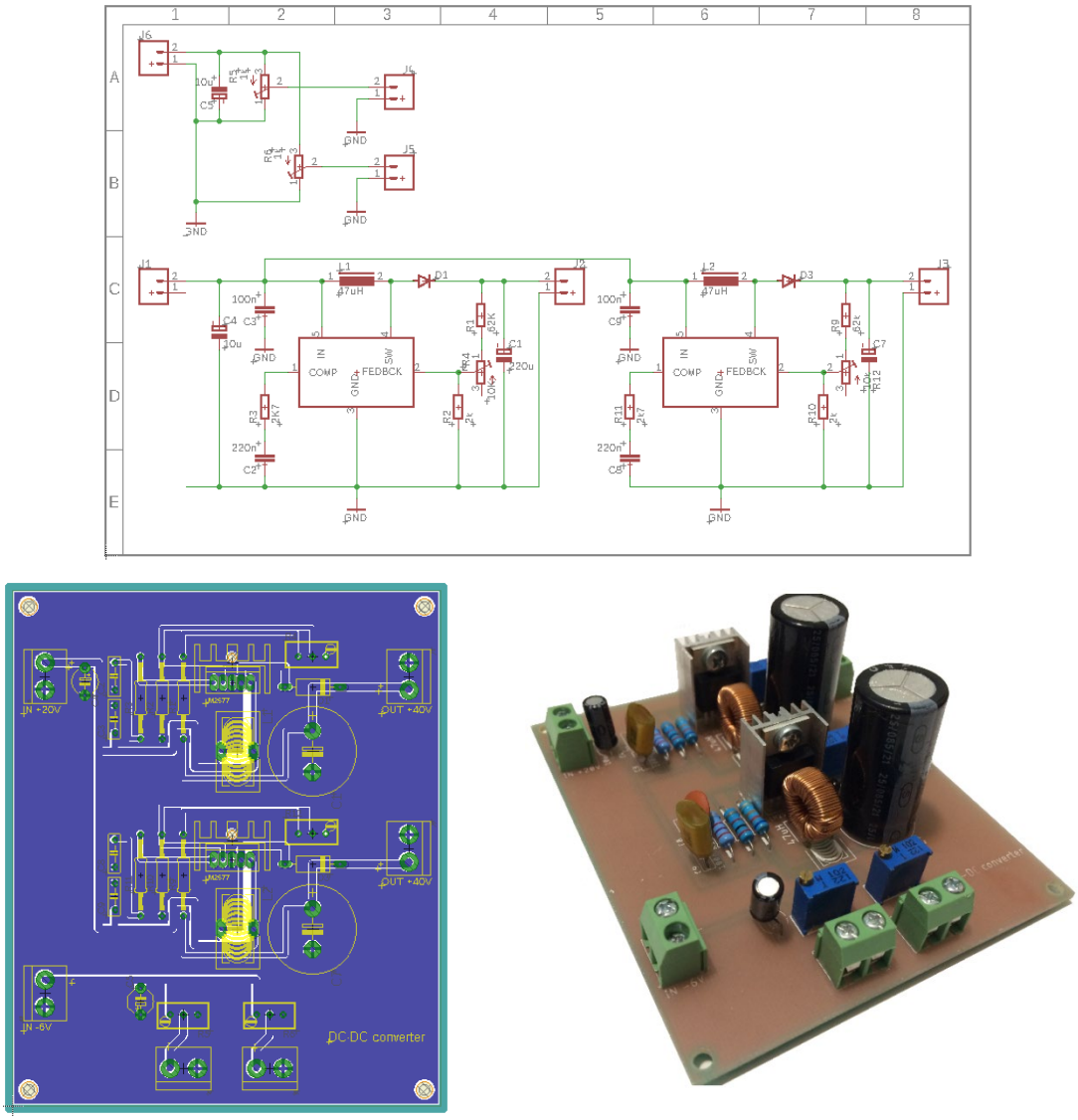


Figure 52 40 V DC-DC converter power supply

3. *Bias Sequencing*

GaN devices are depletion mode devices and therefore require a negative gate voltage while the drain voltage is present to prevent damage. With the gate at V_{GS}= 0 V and with drain voltage present a device will have high current and high-power

dissipation which can permanently damage a device. We should insure that negative gate voltage is always present on the device whenever there is drain voltage present. we should also account for discharge of bypass capacitors on the drain bias feeds which can hold voltage for a time period after the drain power supply voltage is removed. The steps of the turn on and off of the transistor are summarized in the following:

1. Turn ON sequence
    I. Apply pinch-off Voltage to the gate (-3 V)
    II. Apply operating voltage to the drain (40 V)
    III. Adjust the gate voltage to set the operating current (-2.76)
    IV. Turn on the RF signal
2. Turn OFF sequence
    I. Turn off the RF signal
    II. Set voltage gate to pinch-off voltage(-3)
    III. Reduce the drain voltage to zero
    IV. Wait 2 seconds then turn off the gate voltage

4. Block gain and Driver:

We stated in the previous chapter that the block gain and the driver amplifies are needed to rise the signal level to a required level. Also the design and simulation related to them are discussed. The fabricated version of these amplifiers is shown in Fig 53.

The output measured levels are illustrated in Fig 54. It is clear from the measuring results that the gain is decreased as the input frequency is increased. The reason for this is due to two parameters. First of all, the gain block amplifier works up

to 4 GHz. This means that the input frequency reaches the end operating frequency of the gain block amplifier. Secondly, the output level of the signal generator decreases as the output frequency is increased. Even though the signal level is raised up to the desired level for the PA.

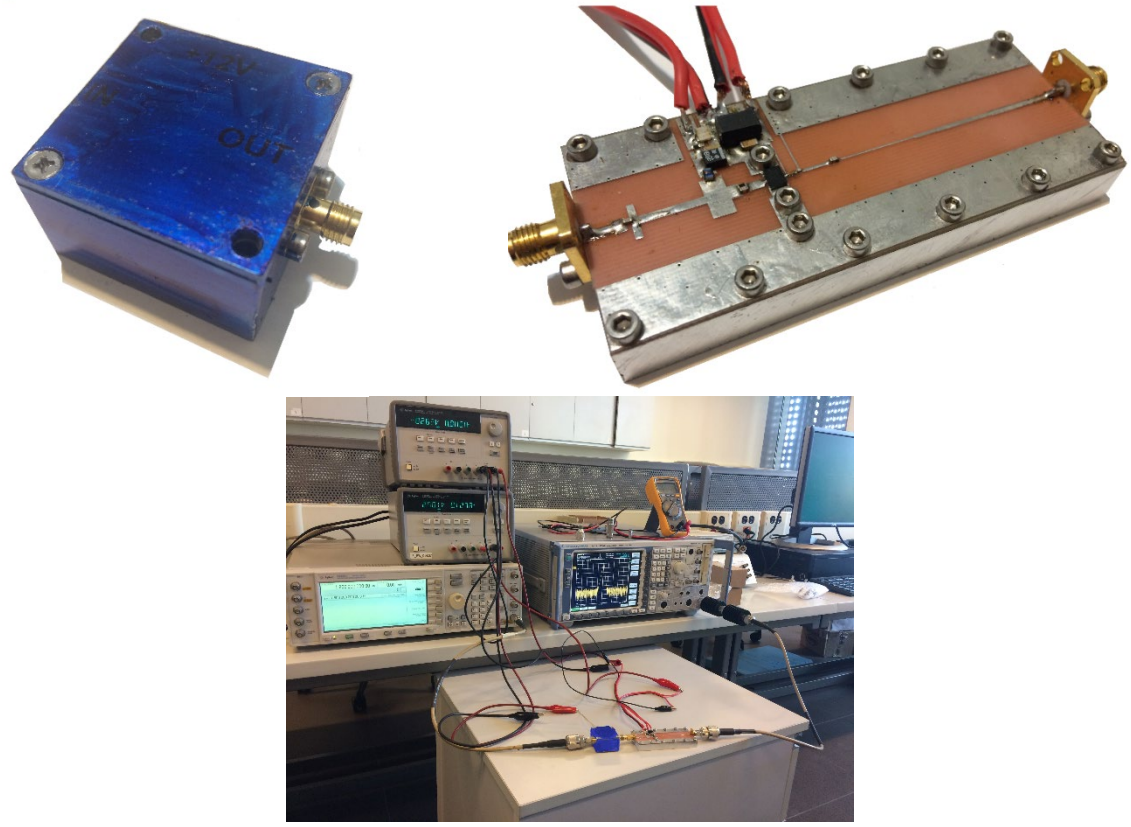


Figure 54 Top left is Block Gain amplifier, top left is Driver amplifier, and bottom is the measurement setup for Gain block-Driver amplifiers

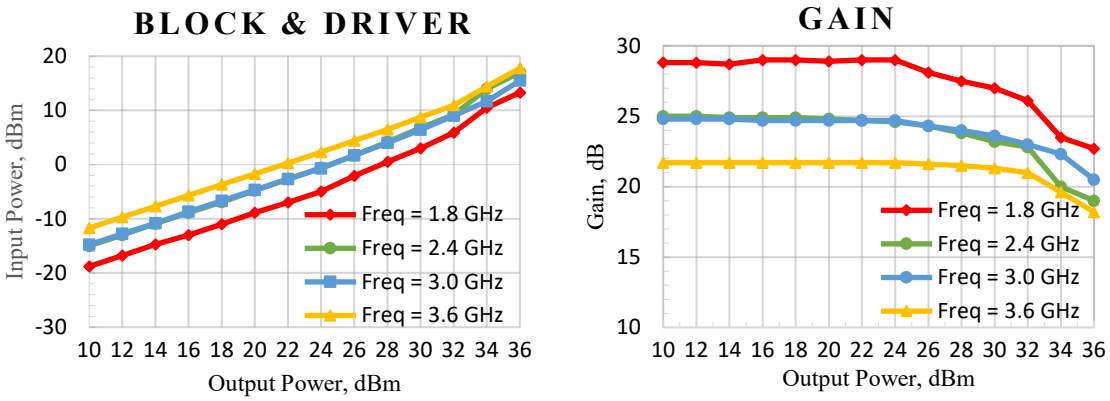


Figure 53 Output power, and gain of the gain block and driver amplifiers

B. Distributed Efficient Power Amplifier DEPA measurement:

Once the required levels are available, the verification measurements for the original design can be established. This step is very important to make a comparison between the simulation results and the actual results. And based on this step, we could make a decision to go forward to fabricate the proposed design or not. The layout, the fabricated design, and the measurement setup of DEPA design are shown in Fig 55

The results are encouraging since the drain efficiency and the output power are somehow matching the simulation results, and the little difference is accepted and expected. The design is tested at 8dB BOP level, which is +31 dBm. These results are plotted in Fig 56

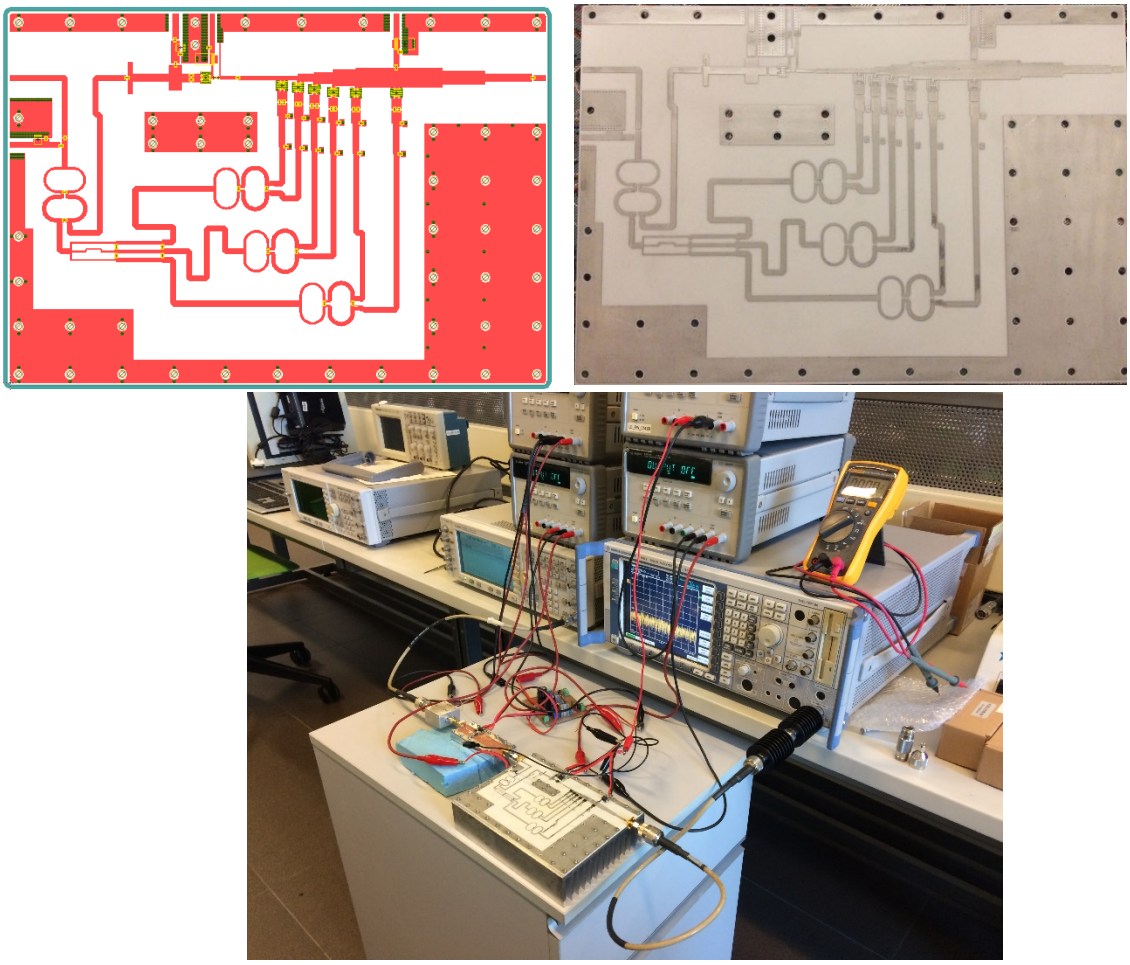


Figure 55 Top left is the DEPA layout, Top right is DEPA fabricated design, Bottom is the measurement setup of the DEAP design

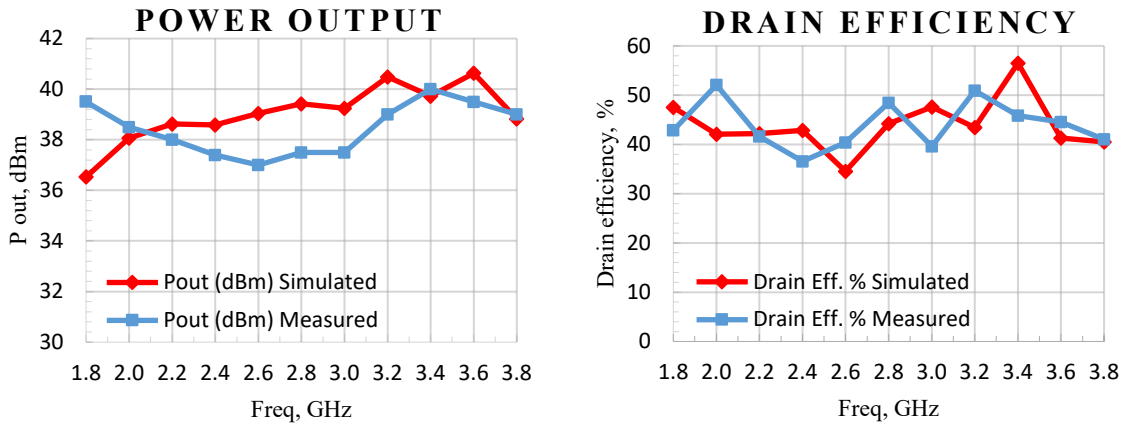


Figure 56 DEPA measurement results

C. Optimized distributed efficient power amplifier measurements:

The proposed amplifier is designed on Rogers 4350B substrate with $\varepsilon_r = 3.55$ and thickness of 32mil. Fig. 56 depicts the layout and the fabricated amplifier. The performance of this PA is tested in small-signal and large-signal conditions.

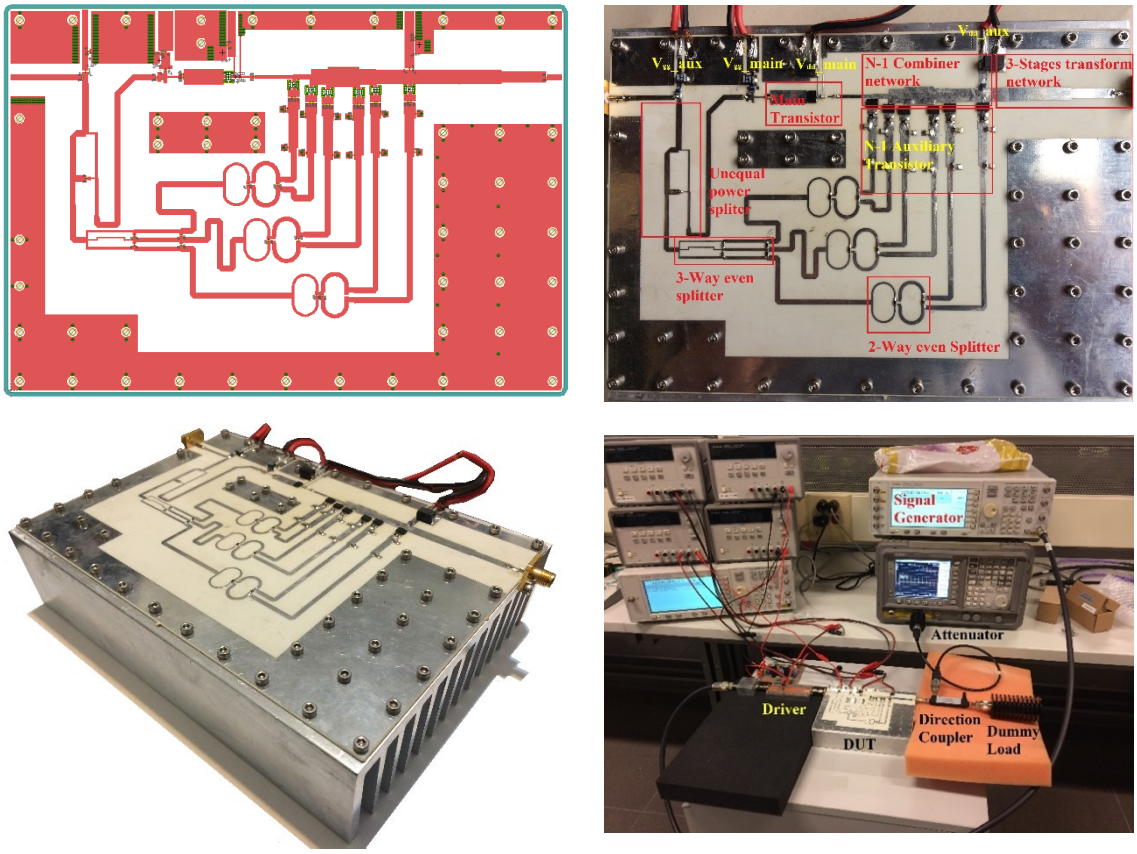


Figure 57 Top left is the ODEPA layout, Top right and bottom left are ODEPA fabricated design, and right bottom is the measurement setup of the ODEAP design

1. Small-Signal Results

The fabricated prototype is tested in a small-signal condition where the main and six auxiliaries are biased at the same drain voltage (40 V). The corresponding quiescent drain current of the main is 20 mA, while the auxiliaries are biased for class-C operation. Fig. 58 depicts the S-parameters results showing a good agreement between the simulation and measured results.

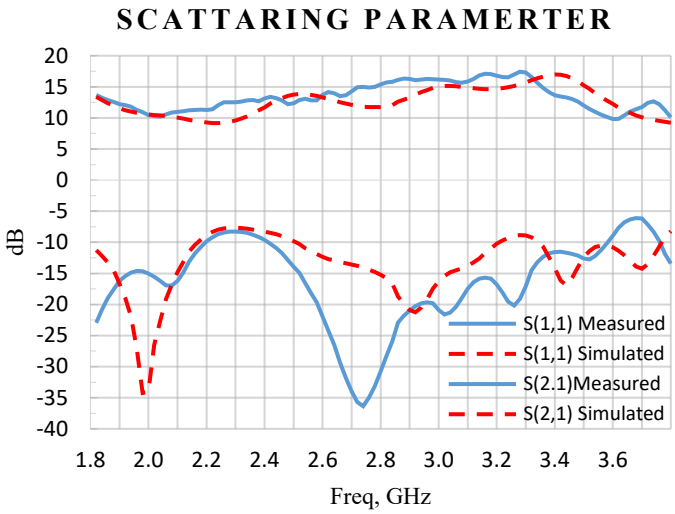


Figure 58 The comparison between the measured and simulated S-parameters

2. Large-Signal Results

Large signal measurements are performed using a continuous wave where the biasing levels are kept the same as the small-signal measurement setup. Fig. 59 shows the simulated and measured output drain efficiency at the peak power and at the 8 dB BOP level. Moreover, the simulated and measured output power of the proposed design at the peak power and at the 8 dB BOP is presented in Fig. 60. It is found that the measured drain efficiency at the BOP level is more than 45 % (i.e., between 45 – 60 %) over the entire span of frequencies (1.8-3.8 GHz).

Finally, the measured gain and drain efficiency of the proposed design as a function of the input power level for different operating frequencies is shown in Fig. 61. All these results prove the outstanding RF performance of the proposed design in comparison to other existing DPA in the literature. Fig. 55 depicts the measurements

setup when characterizing the behaviour of the proposed design using small-signal and large-signal analysis.

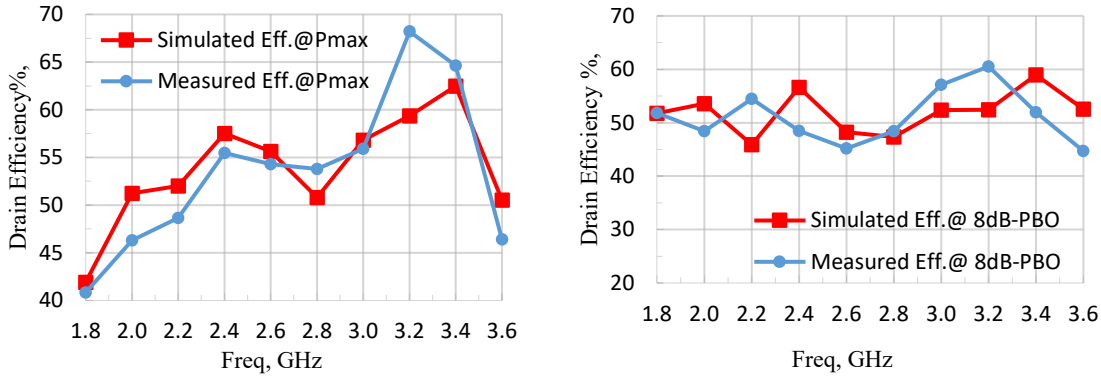


Figure 59 The measured and simulated drain efficiency at the peak power and at the 8dB BOP level

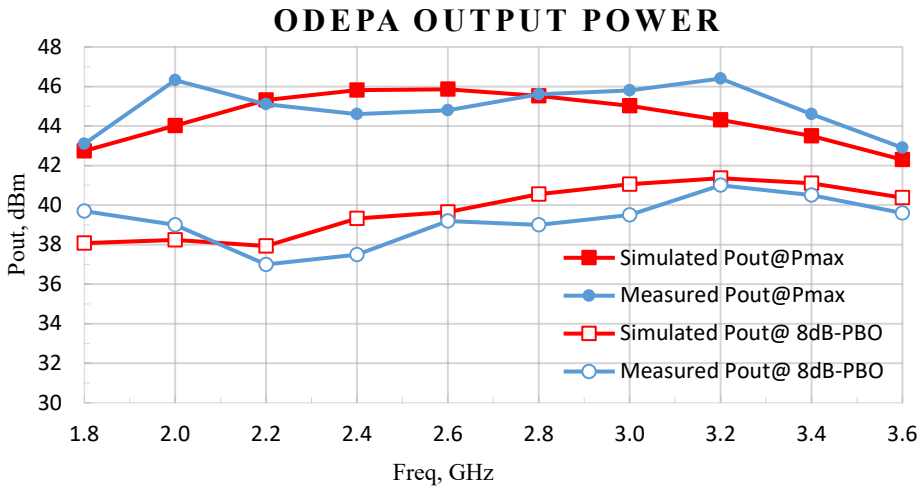


Figure 60 The measured and simulated output power at peak power and BOP levels

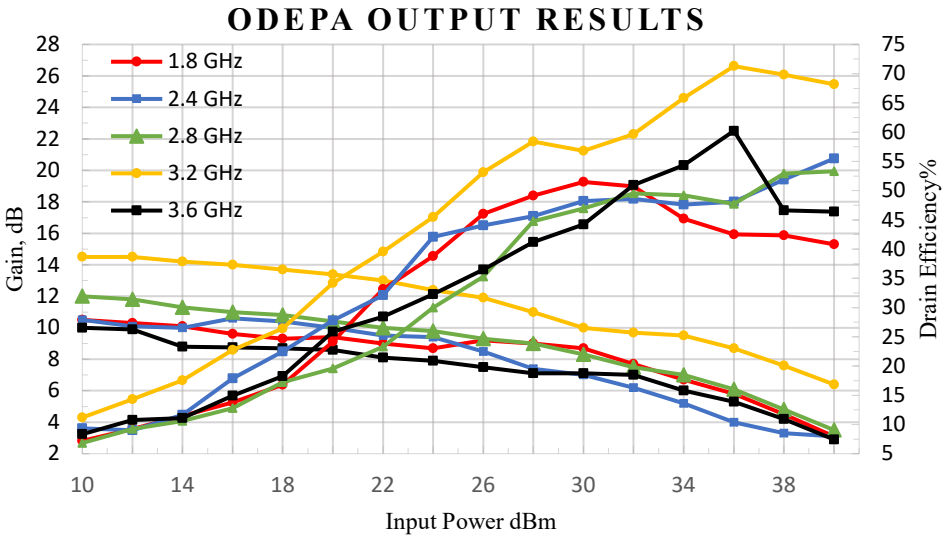


Figure 61 The measured gain and drain efficiency for a span of input power at different operating frequencies

CHAPTER V

CONCLUSION

An optimized broadband PA with a high drain efficiency at a high-power back-off level suitable for PAPR-limited communication systems is presented. The proposed design covers a very wide range of frequencies by eliminating the quarter wavelength bandwidth-limiting factor of classical DPAs. The proposed design is experimentally evaluated by a hardware prototype, thus proving the RF capability of amplifying signals with 8 dB PAPRs. It can be observed from Table 2 that the proposed ODEPA technique advances the state of the art by achieving high efficiency at a large BOP over a very large bandwidth.

Table 2: State-of-the-Art Wideband DPA

Reference	**Freq. (GHz)**	**BW (GHz)**	**FBW (%)**	**BOP dB**	$\boldsymbol{\eta\ BOP}$ **(%)**	$\boldsymbol{\eta\ Peak}$ (%)	**Pout peak (dBm)**
[3]	1.6 – 2.2	0.60	31.6	10	51 – 55	60 – 71	46 – 47
[7]	2.1 – 2.66	0.56	23.5	6	39 – 67	57 – 84	41 – 45
[8]	1.65 – 2.7	1.05	48.3	6	41 – 60	56 – 72	43 – 45
[9]	1.7 – 2.4	0.70	47	6	37 – 48	43 – 54	39.5 – 42
[4]	1.8 – 3.8	2.00	71.5	8	41 – 51	42 – 62	44.3 – 46.5
This work	**1.8 – 3.8**	**2.00**	**100**[1]	**8**	**45 – 60**	**44 – 70**	**43.5 – 64.7**

[1] FBW is defined where higher than 40% efficiency at BOP

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