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RESEARCH PAPER

Microfluidic transistors for analog microflows amplification and control

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Abstract Two microfluidic transistors for analog flow control and amplification for lab-on-a-chip applications are presented. The transistors are based on the elastic membrane microchannel, where the flow in the microchannel between the substrate and the membrane is controlled by the pressure differences along the channel and across the membrane. Reduced-order models that capture the low-inertia dynamic behavior of the coupled fluid–structure interaction were developed to enable fast small-signal analysis of large circuits. The accuracy of the models is assessed by comparing to numerical simulations of the coupled fluid–structure interaction problem. Analog behavior (based on analytical modeling and numerical simulation) of the two devices is characterized in terms of dependence of the volume flow rate on the source–drain and gate–source pressure differences, analogous to the characterization of MOSFET operation. The characteristic curves are then used to extract the small-signal parameters (transconductance and intrinsic output resistance), characterizing the dynamic response to small time-varying pressures at the gate and/or drain. The characterization enabled identification of the various static and dynamic operation regimes of the devices, including the transistive regime where the device operates as amplifier, and the capacitive (positive and negative) regimes. Finally, the dual-membrane transistor is used to showcase its use as a diode and a common-source amplifier in the design of a micropump that, in turn, is used for mixing of two species using pulsating flows.

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List of abbreviations

$\dot{m}$	Mass flow rate
t	Time
f	Frequency
μ	Dynamic viscosity
E	Modulus of elasticity of the gate
A	Cross-sectional area
L	Length of the fluidic transistor channel
L_c	Length of the channel preceding the fluidic transistor
h_0	Reference height of the undeflected transistor channel
W	Width of the fluidic transistor
ρ	Density
d	Thickness of the gate
δ	Vertical deflection of the gate from equilibrium
δ_c	Vertical deflection at the center of the gate
u	Velocity of fluid in the x-direction
U_x	Average velocity of fluid in the x-direction
v	Velocity of fluid in the y-direction
U_y	Average velocity of fluid in the y-direction
w	Velocity of fluid in the z-direction
U_z	Average velocity of fluid in the z-direction
Q	Volume flow rate
g_m	Transconductance
r_o	Intrinsic output resistance
A_v	Intrinsic pressure gain
p	Pressure inside the channel
p_{atm}	Atmospheric pressure
p_{d}	Fluid pressure at the drain

p_s	Fluid pressure at the source
p_g	External gate pressure
$\overline{p}$	Average pressure inside fluidic transistor
p_{sd}	Source–drain pressure drop difference
p_{gs}	Actuation gate pressure relative to source pressure
U_{pois}	Average speed of a Poiseuille flow in a channel of height h_0 due to a reference pressure drop of $p_{sd,0}$
U	Reference speed $= 12U_{pois}$
ν	Kinematic viscosity
$\mathtt{Re}$	Reynolds number
$\mathtt{St}$	Strouhal number
α	Transistor channel aspect ratio
$(.)_0$	Refers to reference or DC state
$(.)_{DC}$	Refers to reference or DC state
$(.)_f$	Refers to fluid
$(.)_m$	Refers to membrane
$(.)_g$	Refers to the gate

1 Introduction

Extensive research has been done on developing and designing microfluidic components and circuits in the last few years, due to the wide spectrum of applications of microfluidic devices, especially in biotechnology.

An important component in such devices is the elastic membrane microchannel, which is made of elastomers, particularly polydimethylsiloxane (PDMS) (Duffy et al. 1998). This component operates as a switch making it the building block of microfluidic logic circuits. Microfluidic logic circuits enable the integration of a large number of components such as valves and pumps, allowing the control of a large number of output flows with a minimal number of input gates, which is essential for saving space and energy (Weaver et al. 2010; Pennathur 2008; Dertinger et al. 2001; Whitesides 2006).

Classically, elastomeric components have been used as basic elements of microfluidic logic circuits. They can act as valves or switches: a pressure difference across the flexible membrane causes a downward deflection that changes its state from open to closed, either allowing the flow to pass or blocking it (Jeon et al. 2002; Toepke 2007; Weaver et al. 2010; Rhee 2009; Oh 2012). The literature is abundant with examples of using elastomeric components as an ON/OFF switching devices.[1] For instance, usage as an active switch can be found in Rhee (2009), Tanaka (2013), whereas usage as a passive switch can be found in Leslie et al. (2009). Elastomeric components are also commonly used as transistors for logic control (switch with gain) of microfluidic circuits (Weaver et al. 2010; Leslie et al. 2009). In addition, elastic membrane equipped channels have been used as diodes (Mosadegh et al. 2011; Jeon et al. 2002) and capacitors (Leslie et al. 2009; Laser 2004) for charging and discharging mass.

Complex devices that employ these basic components include microfluidic oscillators (Mosadegh et al. 2011; Kim 2012), pumps (Leslie et al. 2009; Laser 2004), and frequency-specific mircofluidic control circuits (Leslie et al. 2009).

In the logic (digital) operation of transistors, the designer pays no attention to issues such as nonlinearity and distortion (as long as the device switches between the ON/OFF states in a predictable manner and without failure). One of the advantages for considering analog designs, in addition, is that they offer more functionality. For example, in the design of large integrated microfluidic circuits, when amplifying harmonic pressure signals using logic devices, the amplified output signals look similar to a square wave. An ideal analog amplifier, however, produces a linearly amplified version of the harmonic input signal. In reality, components such as the elastomeric channel are nonideal, and their output suffers from compression and harmonic distortion. One of the benefits and challenges of analog design is to produce an output signal with acceptable gain, linearity, and distortion, while dealing with nonlinear components. None of the previously mentioned studies investigates the analog operation of the elastomeric membrane as a transistor.

In this paper, we first present novel regimes of the elastic membrane microchannel, as a microfluidic transistor for analog flow control and amplification, and as capacitor with positive and negative capacitance. This device, depicted in Fig. 2a, is a single-membrane transistor that consists of a microchannel with a compliant wall where the fluid flow rate is controlled by the combined effect of the pressure differential along the channel ($p_s - p_d$) and the upper wall deflection (δ), controlled by the external pressure (p_g). Second, we present a novel device consisting of two single-membrane units in series, where the external pressure at the membrane of the second unit is the same as the source pressure of the first unit. We demonstrate that this dual-membrane device, depicted in Fig. 2b, not only performs as a better transistor, but can be used a diode (passive) and shutdown safety switch.

Similar designs to our first device are found in the literature (Weaver et al. 2010; Takao et al. 2002; Takao and Ishida 2003; Mosadegh et al. 2011). However, these designs are only used for logic operations, acting as ON/OFF switches with gain. It should be noted here that the authors in Takao et al. (2002), Takao and Ishida (2003) have worked on characterizing (experimentally) the transistive regime of a device similar to our first design, but

[1] In the literature, we noticed a confusion between a diode and a valve. A diode is a passive one-way valve; by passive, we mean that it is actuated by the flow itself. All the others are passive or actively controlled switches.

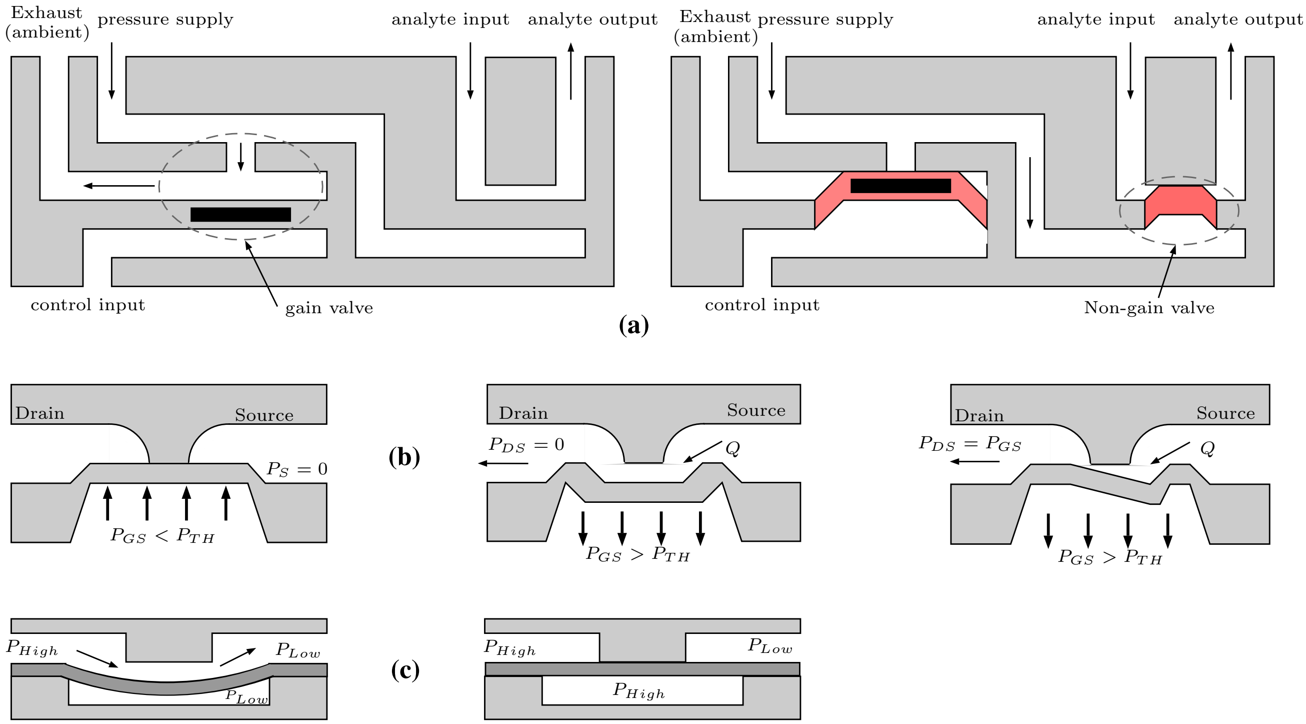


Fig. 1 **a** Control logic using pressure gain valve (Weaver et al. 2010), **b** pneumatic silicon microvalve (Takao et al. 2002; Takao and Ishida 2003), **c** elastomeric switch valve (Mosadegh et al. 2011)

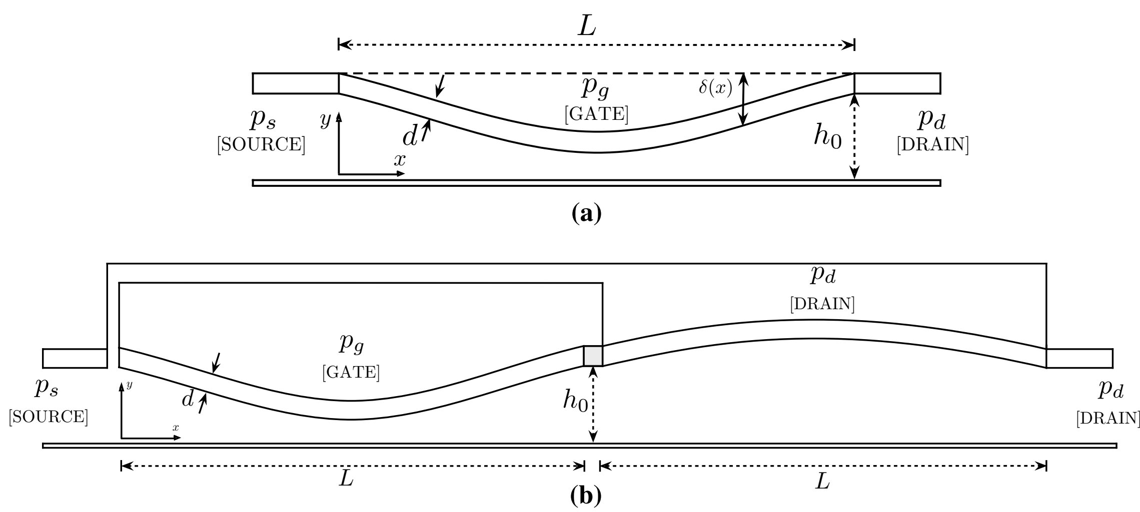


Fig. 2 Schematics of the single- and dual-membrane microfluidic transistors. **a** Single-membrane transistor, **b** dual-membrane transistor

the pneumatic microvalve proposed in these papers is made of silicon, and the membrane is actuated away from the fluidic channel, which is otherwise blocked (see Fig. 1b). Although this device was characterized in a manner similar to that of a pMOS, it was showcased in Takao and Ishida (2003) as a switching device with gain (an inverting amplifier). For a comparison of these various devices, see Fig. 1.

Although elastomeric components can be found frequently in the literature, detailed characterization of the static and dynamic behavior over wide ranges of operating parameters is still lacking. Such an understanding predicts the dynamic dependence of the flow rate on geometric parameters, physical properties, pressure drop along the channel, and the external actuation force. Analogies between electric and fluidic components have been extensively used in fluidic circuit analysis (Oh 2012). The motivation behind this analogy is that the analysis of large networks of fluidic circuits is made simpler by using the well-established techniques in electric circuit analysis. Successful component design requires accurate and fast characterization of the device behavior over the intended regime of operation. Reduced-order models Issa (2015), Issa and Lakkis (2014, 2013), Lakkis (2008) that are cost-effective and accurate can be used to characterize these various components, making it efficient to design and simulate large microfluidic circuits. Another contribution of this work is to present a reduced-order analytical model that captures the low-frequency behavior of the devices shown in Fig. 2. This model is based on coupling the equations governing the membrane deflection and fluid flow in the channel, while employing simplifying assumptions to reduce their complexity.

The paper is organized as follows. The reduced-order model is presented in Sect. 2. Implementation aspects of the model are presented in Sect. 3. In Sect. 4, numerical simulations (Ansys–Fluent) are used for characterizing the device behavior in terms of the dependence of the flow rate Q on the operating pressure differences ($p_{\mathrm{sd}} = p_{\mathrm{s}} - p_{\mathrm{d}}$ and $p_{\mathrm{gs}} = p_g - p_{\mathrm{s}}$). This is done in a manner analogous to the standard characterization of electronic transistors. In addition to the characteristic curves, the reduced-order parameters (i.e., the transconductance, intrinsic output resistance, and pressure gain) are presented over wide ranges of operating pressures. Accuracy of the proposed reduced-order model is assessed by comparing its performance with Ansys fluid–structure interaction (FSI) simulations. In Sect. 5, the behavior of the dual-membrane transistor (Fig. 2b) is discussed and compared to that of a single-membrane transistor (Fig. 2a) in terms of the static and small-signal operations of the devices. Applications of how the transistor can be used are presented in Sect. 6.

2 Reduced-order model of the microfluidic transistor

In this section, a reduced-order model of the single-membrane microfluidic transistor is presented. The model accounts for the coupling between the solid mechanics of the membrane and the fluid dynamics of the channel flow through the pressure distribution in the channel. Various models of a fluidic microchannel with a deformable membrane can be found in the literature (Begley 2008; Senturia 2002; Bakarji et al. 2013). In Begley (2008), the deflection of the membrane is expressed as a fourth-order polynomial as a function of the average pressure differential across the channel. The model assumes a symmetric membrane with no pressure difference across the channel ($p_{\mathrm{sd}} = 0$). A model that accounts for the pressure drop along the channel is presented in Bakarji et al. (2013). The model uses a trial function for the deflection proposed in Senturia (2002) that automatically satisfies the boundary conditions at both fixed ends, and accounts for both small and large deflections (stretching and bending) at the center. The model, however, only allows deflections that obey the trial function, where the maximum deflection is always in the middle (at $L/2$), with the approximation that the pressure distribution on the flow side of the membrane is uniform. These assumptions contribute to significant departure of the behavior predicted by the model from the actual behavior, especially for larger pressure differences along the channel. In what follows, we present an improved model of the single-membrane microfluidic transistor that allows for more accurate membrane deflection and flow pressure profiles along the channel.

2.1 Plate deflection

Considering an isotropic homogeneous thin rectangular plate clamped at its edges, the deformation (measured upward) is governed by (Timoshenko et al. 1959)

$$D\nabla^2\nabla^2\delta + c\frac{\partial\delta}{\partial t} + \rho_m d\frac{\partial^2\delta}{\partial t^2} = p(x,t) - p_{\mathrm{g}} + N_x\frac{\partial^2\delta}{\partial x^2} + N_z\frac{\partial^2\delta}{\partial z^2} - 2N_{xz}\frac{\partial^2\delta}{\partial x\partial z} \tag{1}$$

where

$$\nabla^2\nabla^2\delta = \frac{\partial^4\delta}{\partial x^4} + 2\frac{\partial^4\delta}{\partial x^2\partial z^2} + \frac{\partial^4\delta}{\partial z^4}, \tag{2}$$

$p(x, t)$ is the pressure exerted on the plate by the fluid in the channel, p_{g} is the pressure applied externally on the other side of the plate (gate), δ is the mid-plane deflection in the direction normal to the flow, D is the flexural rigidity ($D \equiv Ed^3/(12(1-\nu^2))$), c is the damping coefficient, ρ_m is the plate density, d is the plate thickness, and N_x, N_z and N_{xz} are the in-plane stretching stresses, expressed, respectively, in terms of the strains as

$$N_x = \frac{Ed}{1-\nu^2}(\epsilon_x + \nu\epsilon_z) \tag{3}$$

$$N_z = \frac{Ed}{1-\nu^2}(\epsilon_z + \nu\epsilon_x) \tag{4}$$

$$N_{xz} = Gd\gamma_{xz} \tag{5}$$

Assuming that the plate width (normal to flow) is much larger than its length (along the flow), $W/L >> 1$, strains in the z-direction can then be neglected, so that $\epsilon_z = 0$ and $\gamma_{xz} = 0$ (plane strain). This implies that the displacement in the z-direction is zero, $\delta_z = 0$, and the displacements in the x- and y-directions do not depend on z, i.e., $\partial\delta_x/\partial z = \partial\delta_y/\partial z = 0$. Using $\delta \equiv \delta_y$,

$$N_x = \frac{Ed}{1-\nu^2}\epsilon_x = \frac{Ed}{1-\nu^2}\left(\frac{\partial\delta_x}{\partial x} + \frac{1}{2}\left(\frac{\partial\delta}{\partial x}\right)^2\right) \tag{6}$$

Upon employing the equations of equilibrium of a differential element in the $x-z$ plane, we get

$$\frac{\partial N_x}{\partial x} = 0 \tag{7}$$

so that the stretching force is independent of x and is expressed as

$$N_x = \frac{Ed}{2(1-\nu^2)L}\int_0^L \left(\frac{\partial\delta}{\partial x}\right)^2 \mathrm{d}x \tag{8}$$

The equation governing the deflection of the plate is then

$$D\frac{\partial^4\delta}{\partial x^4} + c\frac{\partial\delta}{\partial t} + \rho_m d\frac{\partial^2\delta}{\partial t^2} = p - p_\mathrm{g} + N_x\frac{\partial^2\delta}{\partial x^2} \tag{9}$$

Scaling δ by a reference channel height, h_0, x by channel length, L, t by $1/f$, where f is a reference frequency of the forcing (pressure at gate or pressure at drain), p by a reference pressure, p_0, Eq. (9) is expressed in dimensionless form as

$$\frac{\partial^4\hat{\delta}}{\partial\hat{x}^4} + \frac{cfL^4}{D}\frac{\partial\hat{\delta}}{\partial\hat{t}} + \frac{\rho_m df^2L^4}{D}\frac{\partial^2\hat{\delta}}{\partial\hat{t}^2} = \frac{p_0L^4}{Dh_0}(\hat{p}-\hat{p}_g) + 6\frac{h_0^2}{d^2}\left(\int_0^1\left(\frac{\partial\hat{\delta}}{\partial\hat{x}}\right)^2 d\hat{x}\right)\frac{\partial^2\hat{\delta}}{\partial\hat{x}^2} \tag{10}$$

where the hats denote dimensionless quantities. By inspecting Eq. (10), it can be deduced that inertia and damping effects can be neglected when $\frac{\rho_m df^2L^4}{D} << 1$ and $\frac{cfL^4}{D} << 1$ respectively. So if the forcing frequency f is much less than $\sqrt{\frac{D}{\rho_m dL^4}}$ and $\frac{D}{cL^4}$, the effects of inertia and damping can be neglected and the plate can be assumed to instantly respond to pressure loading with a quasi-static deflection profile governed by

$$\frac{\partial^4\hat{\delta}}{\partial\hat{x}^4} - 6\beta^2\left(\int_0^1\left(\frac{\partial\hat{\delta}}{\partial\hat{x}}\right)^2 d\hat{x}\right)\frac{\partial^2\hat{\delta}}{\partial\hat{x}^2} = \Pi(\hat{p}-\hat{p}_g) \tag{11}$$

where $\beta \equiv h_0/d$, $\Pi \equiv \frac{p_0L^4}{Dh_0} = 12(1-\nu^2)\frac{\beta^3 p_0}{\alpha^4 E}$, and $\alpha = h_0/L$. It can be seen from Eq. (11) that for deflections much less than the plate thickness, pure bending dominates stretching, whereas stretching dominates pure bending when the deflection is larger than plate thickness. Note that although structural damping is neglected, the damping force imparted by the fluid on the plate dynamics is present through the coupling of the pressure distribution in the fluid with the viscous shear. The solution of Eq. (11) is

$$\hat{\delta}(\hat{x},\hat{t}) = C_1(\hat{t})\sinh(a\hat{x}) + C_2(\hat{t})\cosh(a\hat{x}) + C_3(\hat{t})\hat{x} + C_4(\hat{t})g(\hat{x}) + C_0(\hat{t}) \tag{12}$$

where

$$\begin{aligned}
C_1 &= \frac{g(1)a\sinh(a) + (1-\cosh(a))g'(1)}{a^2B}\\
C_2 &= \frac{(1-\cosh(a))ag(1) + (-a+\sinh(a))g'(1)}{a^2B}\\
C_3 &= \frac{-a^2g(1)\sinh(a) + (\cosh(a)-1)ag'(1)}{a^2B}\\
C_4 &= \frac{a^2\sinh(a) + 2(1-\cosh(a))a}{a^2B}\\
C_0 &= \frac{(\cosh(a)-1)ag(1) + (a-\sinh(a))g'(1)}{a^2B}\\
B &= 4 + 2a\sinh(a) - 4\cosh(a)
\end{aligned} \tag{13}$$

$$g(\hat{x},\hat{t}) = \int_0^{\hat{x}}\int_0^{x_3}\left(\mathrm{e}^{a(\hat{t})x_2}\left(\int_0^{x_2}\mathrm{e}^{-a(\hat{t})x_1}f(x_1,\hat{t})dx_1\right) - \mathrm{e}^{-a(\hat{t})x_2}\left(\int_0^{x_2}\mathrm{e}^{a(\hat{t})x_1}f(x_1,\hat{t})dx_1\right)\right)\mathrm{d}x_2\mathrm{d}x_3$$

where $g' = \mathrm{d}g/\mathrm{d}\hat{x}$, $f(\hat{x},\hat{t}) = \Pi(\hat{p}(\hat{x},\hat{t}) - \hat{p}_\mathrm{g})$, and the parameter, $a(\hat{t}) = \sqrt{6\beta^2\int_0^1\left(\frac{\partial\hat{\delta}(\hat{x},\hat{t})}{\partial\hat{x}}\right)^2 d\hat{x}}$, is the solution of the nonlinear equation

$$\begin{aligned}
&\int_0^1 C_4g'(\hat{x})\big(C_4g'(\hat{x}) + 2\big(C_1a\cosh(a\hat{x}) + C_2a\sinh(a\hat{x}+C_3)\big)\big)d\hat{x}\\
&+ C_3^2 + C_1C_2a\sinh(a)^2 + \frac{1}{2}(C_1^2+C_2^2)a\cosh(a)\sinh(a)\\
&- 2C_2C_3(1-\cosh(a)) + 2C_1C_3\sinh(a) + \frac{1}{2}(C_1^2-C_2^2)a^2 = \frac{a^2}{6\beta^2}
\end{aligned}$$

Equation (12) constitutes the plate deflection model that yields the deflection for a given gate pressure and flow pressure distribution along the channel.

2.2 Fluid flow in the channel

Coupling between the plate deformation and the fluid flow in the channel is through the pressure distribution in the flow, $\hat{p}$, and the plate deflection, $\hat{\delta}$. On the fluid side, the conservation of mass and momentum for a Newtonian incompressible fluid is governed by the following equations

$$\nabla\cdot\mathbf{u} = 0 \tag{14}$$

$$\rho_f\left(\frac{\partial\mathbf{u}}{\partial t} + \mathbf{u}\cdot\nabla\mathbf{u}\right) = -\nabla p + \mu\nabla^2\mathbf{u} \tag{15}$$

where $\mathbf{u}$ is the velocity vector, ρ_f and μ are, respectively, the density and dynamic viscosity of the fluid. The gravity body force is neglected, as is typical in microflows. For

$h_0 << L$ and $h_0 << W$, the flow may be modeled as two-dimensional in the $x-y$ domain. Scaling t by $1/f$, x by L, y by h_0, p by a reference pressure drop along the channel, $p_{\mathrm{ds},0}$ (so that $\frac{\partial p}{\partial x}$ scales as $\frac{p_{\mathrm{ds},0}}{L}$), and u by $U=\frac{h_0^2}{12\mu}\frac{p_{\mathrm{ds},0}}{L}$ (Note that $U=U_{\mathrm{pois}}$, the average speed of a Poiseuille flow in a channel of height h_0 due to a reference pressure drop of $p_{\mathrm{ds},0}$), the component of the momentum Eq. (15) along the flow direction is expressed in dimensionless form as

$$\mathtt{Re}\left(\mathtt{St}\frac{\partial\hat{u}}{\partial\hat{t}}+\alpha\,\hat{\mathbf{u}}.\hat{\nabla}\hat{u}\right)=-\mathtt{Po}\frac{\partial\hat{p}}{\partial\hat{x}}+\frac{\partial^2\hat{u}}{\partial\hat{y}^2}+\alpha^2\frac{\partial^2\hat{u}}{\partial\hat{x}^2} \tag{16}$$

where $\mathtt{Re}=\frac{U_{\mathrm{pois}}h_0}{\nu_f}$, $\mathtt{St}=\frac{fh_0}{U_{\mathrm{pois}}}$, and $\mathtt{Po}=12$ are, respectively, the Reynolds, Strouhal, and Poiseuille numbers. In what follows, we drop the hats and present models of the channel flow for the cases when the flow is inertia-free and when the flow has some inertia.

2.2.1 *The inertia-free channel flow model*

When inertia effects are negligible ($\mathtt{Re} << 1$ and $\mathtt{Re.St} << 1$) or when the flow is steady ($\partial u/\partial t=0$) and nearly parallel $\alpha << 1$, the momentum equation in the flow direction may be approximated as

$$0\simeq-\mathtt{Po}\frac{\partial p}{\partial x}+\frac{\partial^2 u}{\partial y^2} \tag{17}$$

Since from continuity (14), $v\sim\alpha u$, it can be seen, by comparing the x-component to the y-component of the momentum equation, that $\left|\frac{\partial p/\partial y}{\partial p/\partial x}\right|\sim\alpha$, so that for $\alpha << 1$, $p\simeq p(x,t)$. Integrating Eq. (17), subject to no-slip boundary conditions $u(0)=u(h)=0$, we get

$$u_0=\frac{\eta(1-\eta)h^2\mathtt{Po}}{2}\left(-\frac{\partial p}{\partial x}\right) \tag{18}$$

where $\eta\equiv y/h(x)$ and the subscript 0 denotes inertia-free solution. Expressing $h(x,t)=1+\delta(x,t)$, the volume flow rate (normalized by Uh_0) is then

$$Q_0=(1+\delta)^3\left(-\frac{\partial p}{\partial x}\right) \tag{19}$$

Noting that, from conservation of mass, Q does not vary in x, the flow rate and the pressure distribution along the channel are given by

$$Q_0=p_{\mathrm{sd}}\left(\int_0^1\frac{1}{(1+\delta)^3}\mathrm{d}x\right)^{-1} \tag{20}$$

and

$$p_0=p_{\mathrm{s}}-Q_0\int_0^x\frac{1}{(1+\delta(\chi,t))^3}\mathrm{d}\chi \tag{21}$$

where p_{sd} is the pressure drop along the channel. Equations (20) and (21) constitute the inertia-free model of the channel flow that yields the pressure distribution along the channel and the volume flow rate for a given plate deflection profile, $\delta(x)$, and a given pressure drop, p_{sd}.

2.2.2 *The low-inertia channel flow model*

To account for inertia, the inertia term is estimated from the velocity solution of the inertia-free model, and the pressure distribution and the flow rate are then updated. The continuity equation is used to get an expression for v, with u_0 and p_0, so that

$$v_1=\frac{\mathtt{Po}}{2A(1)}\frac{h'}{h}\eta^2(1-\eta)p_{\mathrm{sd}}$$

where $h'=\mathrm{d}h/\mathrm{d}x$, $A(x)=\int_0^x\mathrm{d}x'/h(x')^3$ and the subscript 1 refers to solution with inertia correction. Note that, from the continuity equation, v is scaled by αU_{pois}. An improved estimate of the pressure can then be obtained from the y-component of the momentum equation, where it is assumed that the pressure term balances the diffusion term (negligible inertia)

$$0\simeq-\mathtt{Po}\frac{\partial p_1}{\partial y}+\alpha^2\frac{\partial^2 v_1}{\partial y^2}$$

which yields

$$p_1\simeq\frac{\alpha^2p_{\mathrm{sd}}}{A(1)}\frac{h'}{h^2}\left(\eta-\frac{3}{2}\eta^2\right)+f(x) \tag{22}$$

where $f(x)=p_1(x,y=0)$ is the pressure distribution at the lower wall. Note also that $p_{\mathrm{s}}=\int_0^1p_1(0,y)\mathrm{d}y$ and $p_{\mathrm{d}}=\int_0^1p_1(1,y)\mathrm{d}y$. An improved solution of u that includes correction for inertia is then determined by solving the steady momentum equation in the flow direction

$$\alpha\mathtt{Re}\left(u_0\frac{\partial u_0}{\partial x}+v_1\frac{\partial u_0}{\partial y}\right)=-\mathtt{Po}\frac{\partial p_1}{\partial x}+\frac{\partial u_1^2}{\partial y^2} \tag{23}$$

The solution of Eq. (23), upon satisfying the no-slip boundary conditions at solid walls, is

$$\begin{aligned}u_1=&\frac{\alpha\mathtt{RePo}^2}{240A(1)^2}\frac{h'}{h}\left(\eta-5\eta^4+6\eta^5-2\eta^6\right)p_{\mathrm{sd}}^2+\frac{\mathtt{Po}}{2}h^2f'\eta(\eta-1)\\&+\frac{\alpha^2\mathtt{Po}}{2A(1)}\left(\left(\frac{h'^2}{h}-\frac{h''}{4}\right)\eta^4-\left(\frac{h'^2}{h}-\frac{h''}{3}\right)\eta^3-\frac{h''}{12}\eta\right)p_{\mathrm{sd}}\end{aligned} \tag{24}$$

where $f'\equiv\mathrm{d}f/\mathrm{d}x$. Noting that $f(0)=p_{\mathrm{d}}$ and $f(1)=p_{\mathrm{s}}$, equation (24) is integrated to get the flow rate as

$$Q_1=Q_0\left[1-\frac{\alpha^2}{10A(1)}\int_0^1\left(\frac{3h'^2}{h^3}+\frac{h''}{2h^2}-\frac{9}{7}\frac{\mathtt{Re}Q_0}{\alpha}\frac{h'}{h^3}\right)\mathrm{d}x\right] \tag{25}$$

The function $f(x)$ can be determined by noting that $Q_1 = \int_0^{h(x)} u_1 \mathrm{d}y$ is independent of x, resulting in the pressure distribution

$$p_1 \simeq p_0 + \alpha^2 Q_0 \left\{ \frac{h'}{h^2}\left(\eta - \frac{3}{2}\eta^2\right) - \frac{1}{10}\int_0^x \left(\frac{3h'^2}{h^3} + \frac{h''}{2h^2} - \frac{9}{7}\frac{\mathrm{Re}Q_0}{\alpha}\frac{h'}{h^3}\right)\mathrm{d}x' + \frac{1}{10}\frac{A(x)}{A(1)}\int_0^1 \left(\frac{3h'^2}{h^3} + \frac{h''}{2h^2} - \frac{9}{7}\frac{\mathrm{Re}Q_0}{\alpha}\frac{h'}{h^3}\right)\mathrm{d}x \right\} \tag{26}$$

Equations (25) and (26) constitute the low-inertia model of the channel flow that yields the pressure distribution along the channel and the volume flow rate for a given plate deflection profile, $\delta(x)$, and pressure drop along the channel, p_{sd}.

2.3 DC operating point

The low-inertia model exhibits a nonlinear dependence of the flow rate on the source–drain and gate–source pressure differences $\hat{p}_{sd}$ and $\hat{p}_{gs}$. The flow rate also depends on Reynolds number of the flow, Re, the structural parameter, Π, and the aspect ratio, α:

$$\hat{Q} = \hat{Q}(\hat{p}_{sd}, \hat{p}_{gs}, \mathrm{Re}, \alpha, \Pi) \tag{27}$$

For a given device geometry, material properties, and reference pressure, $p_{sd,0}$, the dimensionless parameters Re, Π, and α are constant and the flow rate is a function of both p_{sd} and p_{gs};

$$\hat{Q} = \hat{Q}(\hat{p}_{sd}, \hat{p}_{gs}) \tag{28}$$

It should be noted that in some cases, there are two equilibrium values of $\hat{Q}$ for a given $\hat{p}_{sd}$ and a given $\hat{p}_{gs}$. As will be shown in Sect. 4, these two operating points are characterized by different deflection profiles of the plate, different pressure distribution along the channel, and different values of Reynolds number, indicating that the channel flow in one of these two operating points has higher inertia.

At static (steady) conditions, the device operates as a variable resistance controlled by the gate pressure, with the resistance given as

$$\hat{R}(\hat{p}_{sd}, \hat{p}_{gs}) = \frac{\hat{p}_{sd}}{\hat{Q}(\hat{p}_{sd}, \hat{p}_{gs})} \tag{29}$$

Characterization of the dynamic behavior of the device is discussed next.

2.4 Capacitance

The capacitive behavior of the device can be investigated through the dependence of the mass stored in the device on gate–drain and gate–source pressure differences, since the device stores mass due to the compliance of the gate. The stored mass is

$$\hat{m}(\hat{p}_{sg}(\hat{t}), \hat{p}_{dg}(\hat{t})) = \int_0^1 (1 + \hat{\delta}(\hat{x}, t))\mathrm{d}\hat{x}, \tag{30}$$

where $\hat{m} = m/(\rho W L h_0)$, and

$$\frac{\mathrm{d}\hat{m}(\hat{t})}{\mathrm{d}\hat{t}} = \hat{C}_{sg}\frac{\mathrm{d}\hat{p}_{sg}}{\mathrm{d}\hat{t}} + \hat{C}_{dg}\frac{\mathrm{d}\hat{p}_{dg}}{\mathrm{d}\hat{t}} \tag{31}$$

$$\hat{C}_{sg}(\hat{p}_{sg}(\hat{t}), \hat{p}_{dg}(\hat{t})) \equiv \left.\frac{\partial \hat{m}}{\partial \hat{p}_{sg}}\right|_{p_{dg}}, \tag{32}$$

$$\hat{C}_{dg}(\hat{p}_{sg}(\hat{t}), \hat{p}_{dg}(\hat{t})) \equiv \left.\frac{\partial \hat{m}}{\partial \hat{p}_{dg}}\right|_{p_{sg}} \tag{33}$$

where $\hat{C}_{sg}$ is the source–gate capacitance; the increase in the mass stored per unit increase in source–gate pressure difference, while holding the drain–gate pressure difference constant. Similarly, $\hat{C}_{dg}$ is the drain–gate capacitance measuring the increase in the mass stored per unit increase in the drain–gate pressure difference, while holding the source–gate pressure difference constant. If the device is symmetric and $p_{sd} = 0$, we expect $\hat{C}_{sg} = \hat{C}_{gd}$. As will be shown in Sect. 4, there exists an operation region where a negative $\hat{C}_{sg}$ capacitance is observed, indicating a reduction in the mass stored as the source–gate pressure difference is increased, for a given drain–gate pressure difference.

2.5 Small-signal behavior (model)

Small-signal operation of the device is characterized in a manner similar to that of an electronic transistor where the flow rate (current) is controlled by the pressure difference between the source and the drain (source–drain voltage) and the pressure difference between the source and the gate (source–gate voltage). At small frequencies, inertia effects may be neglected, and the device behaves as pressure (voltage)-controlled volume flow rate (current) source. The model presented in the previous section exhibits a nonlinear dependence of the flow rate, $\hat{Q}$, on the source–drain, $\hat{p}_{sd}$, and gate–source pressure differences $\hat{p}_{gs}$.

Small-signal models that assume that the pressure signals experience a small time-varying (AC) component on top of a static operating point (or DC Bias) are commonly used to carry out fast small-signal analysis of complex

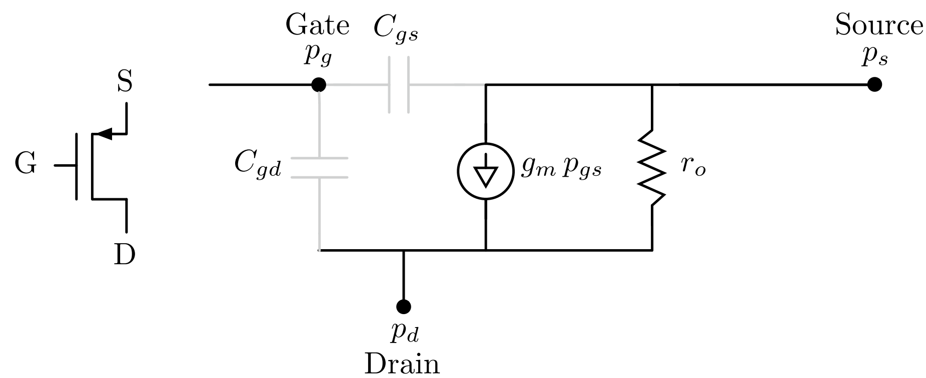


Fig. 3 Small-signal model of the single-membrane microfluidic transistor

electronic circuits. To this end, we express the gate–source pressure difference, source–drain pressure difference, and the volume flow rate as the sum of a steady operating point (DC) component and a small time-varying component,

$$\begin{aligned} p_{\text{gs}}(t) &= p_{\text{gs,DC}} + p'_{\text{gs}}(t) \\ p_{\text{sd}}(t) &= p_{\text{sd,DC}} + p'_{\text{sd}}(t) \\ Q(t) &= Q_{\text{DC}} + Q'(t) \end{aligned} \tag{34}$$

where $|p'_{\text{gs}}/p_{\text{gs,DC}}| << 1$, $|p'_{\text{sd}}/p_{\text{sd,DC}}| << 1$, and $|Q'/Q_{\text{DC}}| << 1$. For a given device geometry, material properties, and reference pressure $p_{\text{sd},0}$, the dimensionless parameters $\mathtt{Re}$, Π, and α are constant and the flow rate is a function of both p_{gs} and p_{sd}, so that

$$\mathrm{d}Q = \left.\frac{\partial Q}{\partial p_{\text{gs}}}\right|_{p_{\text{sd}}} \mathrm{d}p_{\text{gs}} + \left.\frac{\partial Q}{\partial p_{\text{sd}}}\right|_{p_{\text{gs}}} \mathrm{d}p_{\text{sd}} \tag{35}$$

It can then be shown that a linear relationship among the small-signal components is obtained as

$$Q'(t) \simeq g_m p'_{\text{gs}}(t) + \frac{1}{r_o} p'_{\text{sd}}(t) \tag{36}$$

The small-signal behavior is expressed in Eq. (36) in a manner that is analogous to that of electronic MOSFET, where g_m and r_o are, respectively, the transconductance and intrinsic output resistance

$$g_m = \left.\frac{\partial Q}{\partial p_{\text{gs}}}\right|_{(p_{\text{sd}}, p_{\text{gs}})_{\text{DC}}} \tag{37}$$

$$r_o = \left(\frac{\partial Q}{\partial p_{\text{sd}}}\right)^{-1}_{(p_{\text{sd}}, p_{\text{gs}})_{\text{DC}}} \tag{38}$$

In dimensionless form,

$$g_m = \frac{Wh_0^3}{12\mu L}\left(\frac{\partial \hat{Q}}{\partial \hat{p}_{\text{gs}}}\right) = \frac{Wh_0^3}{12\mu L}\hat{g}_m \tag{39}$$

$$r_o = \frac{12\mu L}{Wh_0^3}\left(\frac{\partial \hat{Q}}{\partial \hat{p}_{\text{sd}}}\right)^{-1} = \frac{12\mu L}{Wh_0^3}\hat{r}_o \tag{40}$$

The intrinsic small-signal pressure gain, defined as $A_v = p'_{\text{ds}}/p'_{\text{gs}}$, is given by the product

$$A_v = -\hat{g}_m \hat{r}_o \tag{41}$$

The intrinsic gain is the maximum gain that can be achieved using a single transistor. The small-signal model of the low-inertia behavior is described by the circuit shown in Fig. 3. The model corresponds to a pressure (voltage)-controlled flow rate (current) source in parallel with intrinsic output resistance r_o. The source–gate and drain–gate capacitances, shown in the circuit, can be ignored when the frequency is sufficiently small.

Alternatively, we may express

$$\hat{Q}' = \hat{g}'_m \hat{p}'_{\text{dg}} + \frac{1}{\hat{r}'_o}\hat{p}'_{\text{sd}} \tag{42}$$

where it can be shown that

$$\hat{g}'_m = -\,\hat{g}_m \tag{43}$$

$$\hat{r}'_o = \left(\frac{1}{\hat{r}_o} - \hat{g}_m\right)^{-1} \tag{44}$$

If p^*_{g} is the characteristic gate gage pressure at which the gate closes when the gage pressure in the channel is 0, then

$$\hat{p}^*_{\text{gd}} = \frac{(p_{\text{g}} - p^*_{\text{g}}) - p_{\text{d}}}{p_0} \tag{45}$$

$$\hat{p}^*_{\text{gs}} = \frac{(p_{\text{g}} - p^*_{\text{g}}) - p_{\text{s}}}{p_0} \tag{46}$$

Numerical implementation of the model, along with determination of the capacitances and the small-signal parameters, is discussed in the following section. Discussion of the different operation regimes, predicted by the model

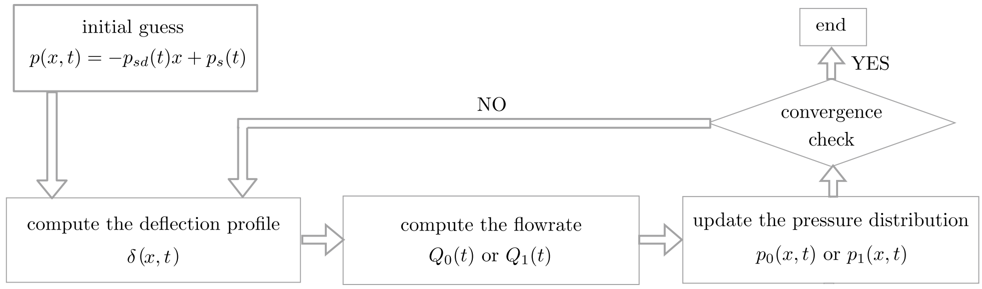


Fig. 4 Flowchart of model implementation

as well as by the detailed computational simulation of the fluid–structure interaction problem, is presented in Sect. 4.

3 Model implementation

The model presented in the previous section enables fast computation of the membrane deflection (Eq. 12), fluid flow rate (Eq. 19 or 25), and pressure distribution along the channel (Eq. 21 or 26) using the following simple iterative method. The method starts by assuming an initial linear pressure profile along the channel similar to that of a Poiseuille flow,

$$\hat{p}(x) = -\hat{p}_{\mathrm{sd}}\hat{x} + \hat{p}_{\mathrm{s}}. \tag{47}$$

The pressure is then plugged in Eq. (12) to get a deflection profile $\hat{\delta}(x)$ of the membrane. The deflection profile is then inserted in the flow rate Eqs. (19) and (25) to determine the flow rate, $\hat{Q}$. The flow rate is then used in Eqs. (21) and (26) to update the pressure profile of the flow under the membrane. This process, illustrated in Fig. 4, is repeated until the solution is converged. The capacitances and the small-signal parameters (transconductance and intrinsic resistance) are determined by numerically computing the derivatives in Eqs. (32), (33), (37), and (38).

4 The single-membrane transistor

In this section, we characterize the behavior of the 2D pressure-actuated single-membrane microfluidic transistor depicted in Fig. 2a, using model-based and fluid–structure interaction (FSI) numerical simulations on FLUENT/Ansys over ranges of operating pressures ($p_{\mathrm{sd}} = p_{\mathrm{s}} - p_{\mathrm{d}}$ and $p_{\mathrm{gs}} = p_{\mathrm{g}} - p_{\mathrm{s}}$). This behavior is presented in the form of characteristic curves similar to those relating the source–drain current to source–drain and gate–source voltage differences in a MOSFET. These characteristic curves are then used as the basis for choosing the static operating point (DC bias) of the transistor and for the extraction of the capacitances and the small-signal parameters such

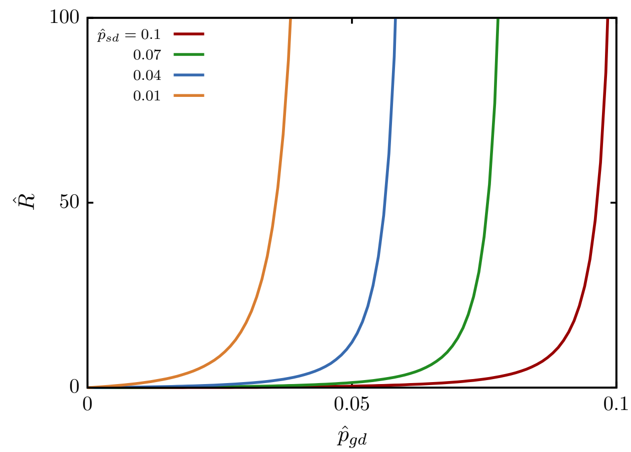


Fig. 5 Static resistance of the single-membrane microfluidic transistor switches from a small value (ON state) at small $\hat{p}_{\mathrm{gd}}$ to a large value (OFF state) at large $\hat{p}_{\mathrm{gd}}$

as transconductance, intrinsic output resistance, and pressure gain. The large-signal steady (DC) behavior as well as the small-signal unsteady (AC) behavior will be qualitatively compared to and contrasted with those of a standard MOSFET.

As depicted in Fig. 2a, the membrane is fixed from both sides ($x = 0$ and $x = L$). For the FSI simulations of the single-membrane transistor, the following dimensions are used: length of the membrane $L = 3118\,\mu$m, the (undeformed) channel height is $h_0 = 59\,\mu$m, the width is $L_z = 500\,\mu$m, and the membrane thickness is $d = 196\,\mu$ m. These dimensions are similar to those used for the fluidic capacitor presented in Leslie et al. (2009). To ensure a fully developed flow at the inlet of the transistor, an entry section is added at the source side of the transistor with a length of $L_e = 600\,\mu$m and height $h_e = h_0 = 59\,\mu$m. The boundary condition at the entry section is prescribed in terms of a velocity inlet and assumed to be uniform. At the outlet, atmospheric pressure is prescribed, i.e., $p_{\mathrm{d}} = p_{\mathrm{atm}}$. A uniform gate pressure, p_{g}, is imposed as a boundary condition in the structural part of the numerical solver.

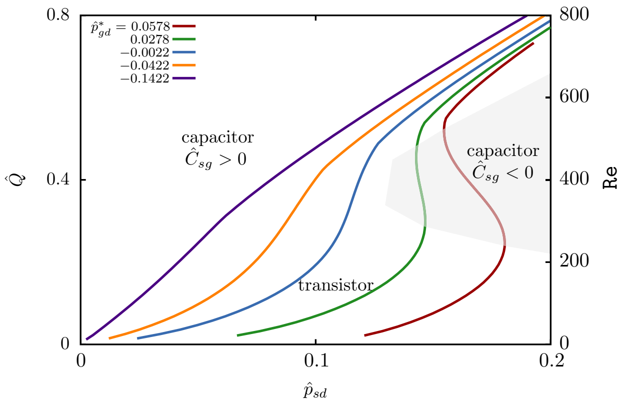


Fig. 6 Characteristic curves of the single-membrane microfluidic transistor computed from numerical simulations of the FSI problem using Ansys

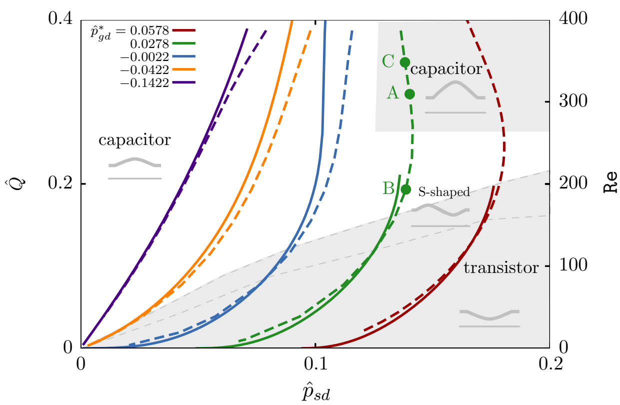


Fig. 7 Characteristic curves of the single-membrane microfluidic transistor. *Solid lines* model. *Dashed lines* Ansys FSI

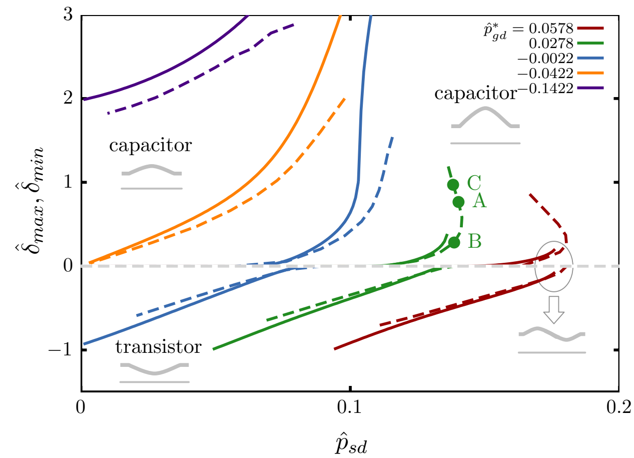


Fig. 8 Plate maximum and/or minimum deflection. Positive indicates upward deflection, and negative indicates downward deflection. *Solid lines* model. *Dashed lines* Ansys FSI

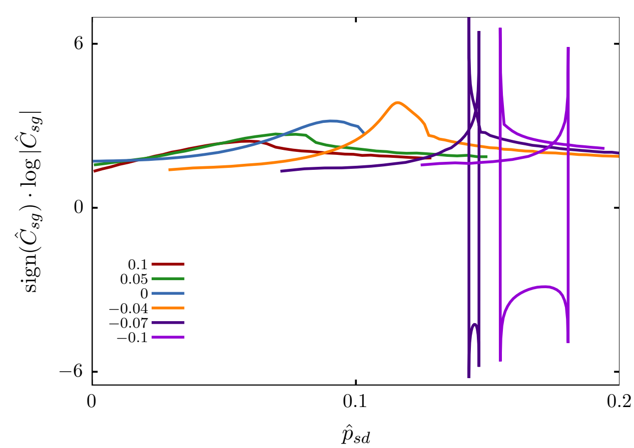


Fig. 9 Source–gate capacitance of the single-membrane device versus source–drain pressure difference for different values of the source–gate pressure difference. *Solid lines* Ansys FSI

The numerical results are obtained from 2D Ansys numerical simulations of the coupled fluid–structure interaction. The simulation mesh is made of cubic elements having a maximum size of 5 µ*m*, with the mesh size chosen so that the solution is nearly mesh-independent. In the solid mechanics part, the computational element is defined by eight nodes with three degrees of freedom at each node. These elements are mainly used for creep, swelling, stress stiffening, large deflection, and large strain simulations.

4.1 Operating point (DC) characteristic curves

At static (steady) operation, the device behaves as a switch controlled by the gate pressure, with the resistance given by Eq. (29). It can be observed from Fig. 5 that, for a given source–drain pressure difference, the resistance increases as the gate pressure is increased, as predicted by the reduced-order model. This is because increasing the gate pressure causes a downward deflection of the plate, thus reducing the channel height, which significantly increases the resistance. One can see that the device at static conditions operates similar to the electric transistor, which has a high resistance when operating in the linear (ohmic) regime and a lower resistance in the saturation regime.

Following the procedure conventionally used in small-signal characterization of electronic transistors (Sedra 2004), a plot of the volume flow rate, $\hat{Q}$, versus the source–drain pressure difference, $\hat{p}_{\mathrm{sd}}$, for different values of the gate–drain pressure, $\hat{p}^*_{\mathrm{gd}}$, is presented in Fig. 6, as predicted by Ansys FSI simulations. Comparison with the model is shown in Fig. 7, where the solid lines denote the flow rates predicted by the model and the dashed line denotes those computed from Ansys FSI simulations. It can be observed

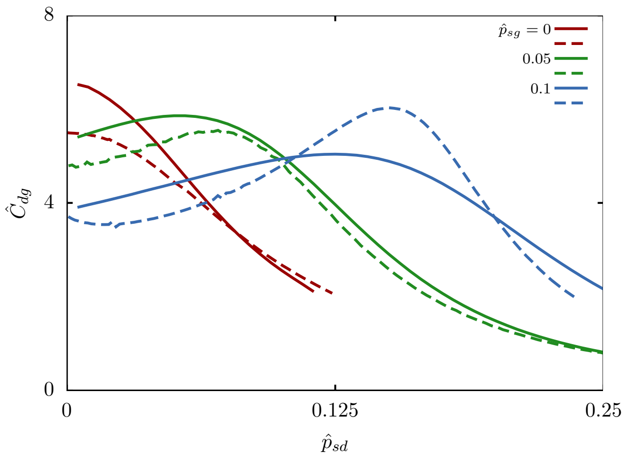


Fig. 10 Drain–gate capacitance of the single-membrane device. *Solid lines* model. *Dashed lines* Ansys FSI

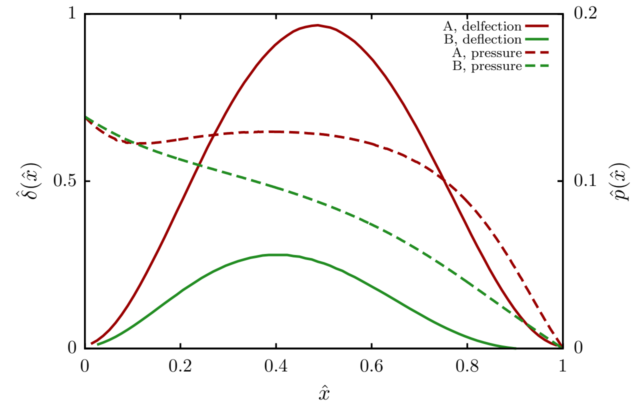


Fig. 11 Deflection and pressure profile for points A and B, shown in Figs. 7 and 8

from the figure that the model is more accurate at smaller values of $\hat{p}_{sd}$ for a given $\hat{p}^*_{gd}$, as inferred by the agreement with the Ansys FSI solution. This is expected because the model is developed for low-inertia flows.

The normalized maximum and/or minimum membrane deflections are plotted in Fig. 8, for the same ranges of $\hat{p}_{sd}$ and $\hat{p}^*_{gd}$ as in Fig. 7. By inspecting Figs. 7 and 8, the following regions of dynamic operation are identified: (1) positive capacitance regime (upward plate deflection), (2) negative capacitance regime (upward plate deflection with significant inertia role), and (3) a transistor region (downward or S-shaped plate deflection). The regimes of dynamic operation are discussed next.

4.2 Capacitive region

The capacitive region is characterized by an upward deflection of the membrane which occurs when $\hat{p}_{sd} > \hat{p}^*_{sd}$, where $\hat{p}^*_{sd}$ is some characteristic source–drain pressure difference. In this region, increasing the source–drain pressure difference, for a given gate–drain pressure difference, causes the plate to deflect further upward so that more mass is stored and the source–gate capacitance is positive; $\hat{C}_{sg} > 0$. The characteristic source–drain pressure difference, $\hat{p}^*_{sd}$, above which the device enters the capacitive region exhibits a linear dependence on the gate–source pressure difference, $\hat{p}^*_{sd} = 1.3\hat{p}_{gd} + 0.05$, as predicted by Ansys FSI simulations.

The dependence of the source–gate and drain–gate capacitances on the source–gate and source–drain pressure differences is presented in Figs. 9 and 10. Upon inspecting these figures, the following observations can be made: (1) the source–gate capacitance is, to a large degree, independent of the source–drain and source–gate pressure differences for smaller positive values of $\hat{p}_{sg}$ and small positive values of $\hat{p}_{sd}$ (e.g., $\hat{C}_{sg} \simeq 6.5 \pm 1$ for $\hat{p}_{sd} < 0.05$ and $\hat{p}_{sg} = 0$), (2) the source–gate capacitance can be increased by decreasing the source–gate pressure while increasing the source–drain pressure up to a point, at which $\hat{C}_{sg}$ is a maximum and beyond which it starts decreasing, (3) for sufficiently large gate–source pressure (e.g., $\hat{p}_{sg} \leq -0.07$, the source–gate capacitance experiences sharp drops from large positive values to large (in absolute value) negative values and vice versa as the flow rate is continuously increased (in addition to Fig. 9, refer to Figs. 6, 7, 8).

It is observed in some cases that, for given source–drain and gate–drain pressure differences, there exist two separate operating points, such as points A and B in Fig. 7. Point A is characterized by a larger flow rate (large Re) and larger upward deflection than point B, as can be observed in Fig. 11. The large deflection at point B is, in part, sustained by a larger pressure in the channel caused by expansion of the flow in the larger channel. In effect, the large upward deflection and the corresponding pressure recovery in the channel enhance one another. Point A belongs to a negative capacitance region. This can be illustrated further by inspecting points A and C in Fig. 8. While both points have the same gate–drain pressure difference, point C is characterized by a larger upward deflection and a smaller source–drain pressure difference when compared to point A, which implies that more mass is stored as the operating point is moved from A to C while the source–drain pressure difference has decreased, indicating that the source–gate capacitance is negative.

4.3 Transistive region

When the plate deflection is downward or when it assumes an S-shape (where it is upward on the source side and downward on the drain side), the device behaves as a transistor that is capable of amplifying small gate pressure variations. As an amplifier, the device can be employed in a common-drain or a common-source configuration, as depicted in Fig. 12.

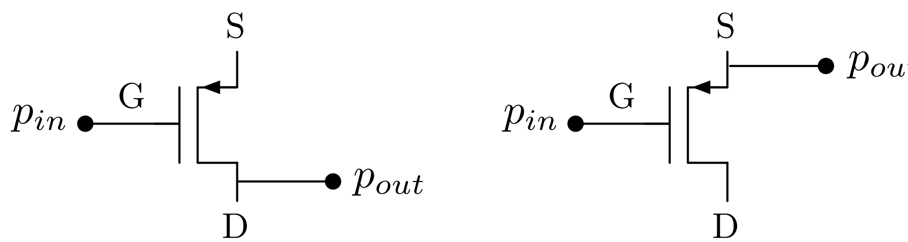


Fig. 12 *Left* common-source configuration. *Right* common-drain configuration

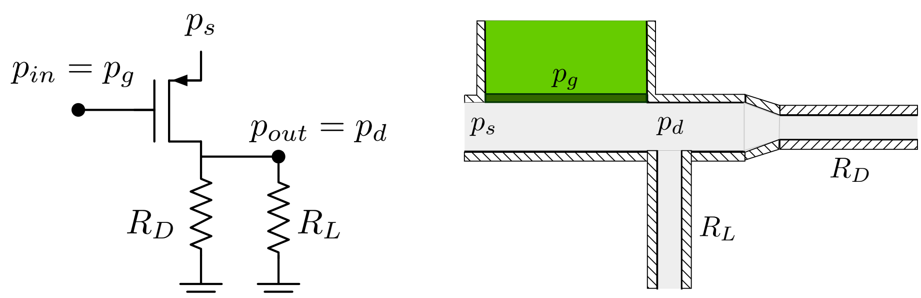


Fig. 13 Single-membrane device in a common-source configuration

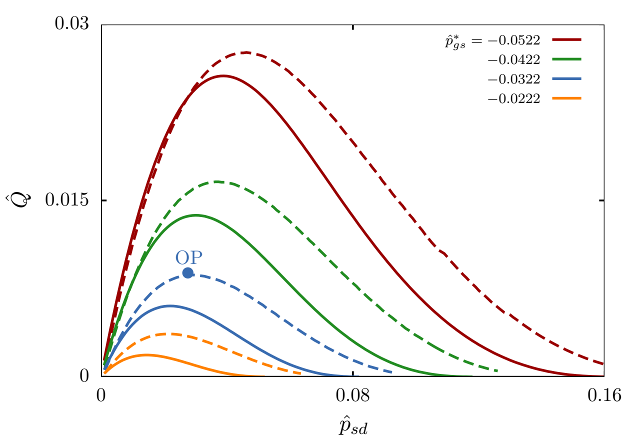


Fig. 14 Characteristic *curves* of the (common-source) single-membrane microfluidic transistor. *Solid Lines* model. *Dashed lines* Ansys FSI

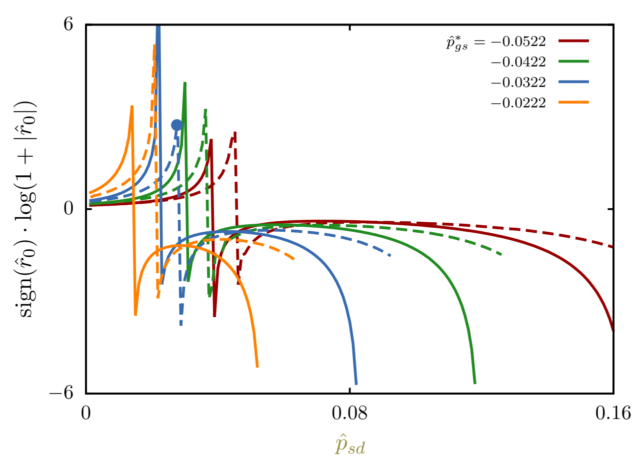


Fig. 15 Intrinsic output resistance of the (common-source) single-membrane microfluidic transistor. *Solid Lines* model. *Dashed lines* Ansys FSI

In electronic circuits, the common-source amplifier, depicted in Fig. 13(left), is commonly used as a voltage amplifier. The input signal voltage is applied at the gate of the MOSFET, and the amplified output voltage is experienced at the drain. In the common-source configuration of the single-membrane microfluidic transistor, shown in Fig. 13(right), the resistance R_D and the load resistance, R_L, are realized by microfluidic channels, and the output is sensed at the drain and the intrinsic small-signal gain is $A_v = \frac{p_{\mathrm{ds}}}{p_{\mathrm{gs}}} = -g_m r_o$. In the common-drain configuration, the output is sensed at the source an intrinsic pressure gain $A'_v = \frac{p_{\mathrm{sd}}}{p_{\mathrm{gd}}} = -g'_m r'_o$.

The single-membrane device has some similarity to a p-type MOSFET, as can be inferred from Fig. 14, where the source–drain flow rate is plotted against the source–drain pressure, $\hat{p}_{\mathrm{sd}}$, for different values of the gate–source pressure, $\hat{p}^*_{\mathrm{gs}} = \frac{(p_{\mathrm{g}} - p^*_{\mathrm{g}}) - p_{\mathrm{s}}}{p_0}$, where $p^*_{\mathrm{g}} = 4220$ Pa is the gate gage pressure at which the channel closes when the drain and source are kept at zero gage pressures.

Similar to its electronic counterpart, the single-membrane microfluidic transistor exhibits a linear dependence of the flow rate on the source–drain pressure difference for small values of this difference; $\hat{p}_{\mathrm{sd}} << |\hat{p}^*_{\mathrm{gs}}|$. This linear (ohmic) regime is followed by a nonlinear regime in which the intrinsic output resistance (inverse of the slope) starts increasing as $\hat{p}_{\mathrm{sd}}$ is increased until it reaches infinity at $\hat{p}^*_{\mathrm{sd}} \simeq 0.837|\hat{p}^*_{\mathrm{gs}}| + 0.019$. The regime in which the incremental output resistance is very large ($\hat{p}_{\mathrm{sd}} \simeq \hat{p}^*_{\mathrm{sd}}$) is called the saturation regime. There is, however, a significant

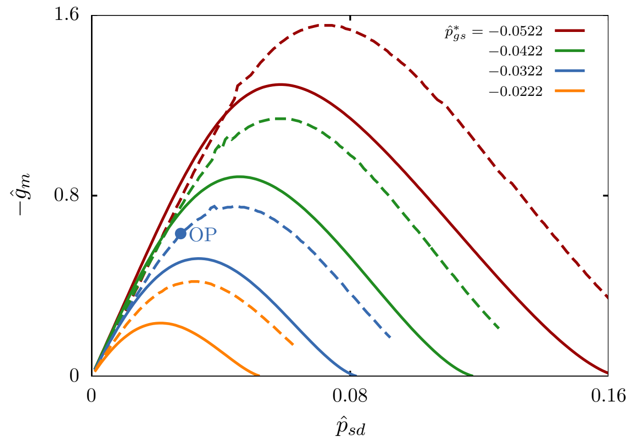


Fig. 16 Transconductance of the (common-source) single-membrane microfluidic transistor. *Solid Lines* model. *Dashed lines* Ansys FSI

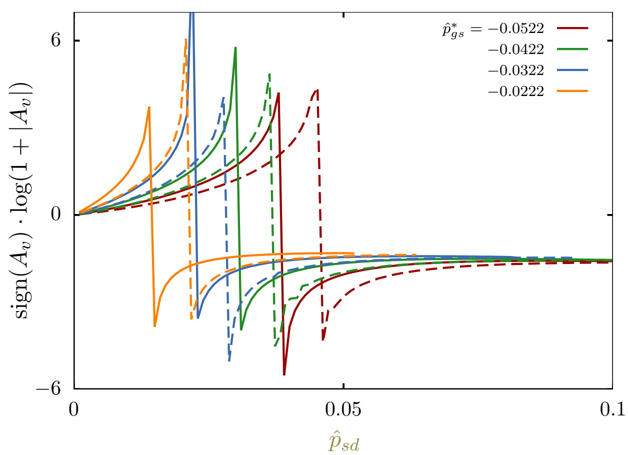


Fig. 17 Gain (unloaded) of the (common-source) single-membrane microfluidic transistor. *Solid Lines* model. *Dashed lines* Ansys FSI

difference between this device and the electronic MOSFET. The saturation region in the MOSFET extends for $V_{\mathrm{sd}} > V^*_{\mathrm{sd}}$ with a very large, ideally infinite, incremental output resistance. In contrast, the saturation regime of the single-membrane microfluidic transistor is limited to a narrow range of the source–drain pressure centered at $\hat{p}^*_{\mathrm{sd}}$, and for $\hat{p}_{\mathrm{sd}} > \hat{p}^*_{\mathrm{sd}}$, the flow rate decreases, indicating a switch in the sign of the output resistance, $\hat{r}_o$ (from positive to negative) accompanied by a reduction in its absolute value. The fact that $\hat{r}_o > 0$ over the entire operation range of the source–drain voltage in a MOSFET is what makes the gain of the common-drain configuration less than unity; $g_m/(1/r_o + g_m) \leq 1$.

This observed dependence of the flow rate on the source–drain pressure as the gate–source pressure is fixed is the outcome of two opposing mechanism. While increasing the source–drain pressure tends to increase the flow rate, it also implies reducing the drain pressure (while keeping the source pressure constant) which pulls the gate into the channel thus reducing the channel height, which in turn reduces the flow rate. For $\hat{p}_{\mathrm{sd}} < \hat{p}^*_{\mathrm{sd}}$, the first mechanism is dominant while in for $\hat{p}_{\mathrm{sd}} > \hat{p}^*_{\mathrm{sd}}$, the second mechanism is dominant.

4.3.1 *Small-signal model parameters*

Characterization and subsequent investigation of the small-signal low-frequency (inertia-free) behavior of the transistor are based on plots of the intrinsic output resistance, the transconductance, and the pressure gain versus $\hat{p}_{\mathrm{sd}}$ for different values of $\hat{p}^*_{\mathrm{gs}}$. These plots are shown in Figs. 15, 16, and 17, respectively. Since the incremental output resistance is the inverse of the slope of the $\hat{Q} - \hat{p}_{\mathrm{ds}}$, $\hat{r}_o$ is singular when $\hat{Q}$ is maximum ($\partial\hat{Q}/\partial\hat{p}_{\mathrm{sd}} = 0$) and switches sign from positive to negative as the flow rate rises to its maximum and then falls as the source–drain pressure is increased from 0. For a given gate–source pressure, the transistor shuts down at high values of the source–drain pressure. This is because for a fixed source pressure, increasing the source–drain pressure is accomplished by reduction in the drain pressure, which causes the membrane to be deflected into the channel, eventually closing it. This effect is expected to be more pronounced at larger values of the Reynolds number, i.e., higher inertia flows. This is because the flow speeds up in the channel region where the membrane deflection into the channel is largest, which in turn reduces the pressure. As the channel closes due to sufficiently low pressure, the incremental output resistance starts approaching $-\infty$, which is the resistance when the channel is closed.

The transconductance, which measures the incremental increase in the flow rate caused by an incremental increase in the gate–source pressure, while holding the source–drain pressure fixed, is negative because increasing the gate pressure reduces the channel height and consequently the flow rate. The transconductance behaves similar to the flow rate, as can be observed from Fig. 16.

These trends of the dependence of $\hat{g}_m$ and $\hat{r}_o$ on $\hat{p}_{\mathrm{sd}}$ produce the pressure gain (Eq. (41)) shown in Fig. 17. The unloaded small-signal gain, A_v, is directly proportional to the incremental output resistance and is therefore singular at the same values of $\hat{p}_{\mathrm{sd}}$ at which $\hat{r}_o$ is singular. Note that relatively large gain realized at large values of $\hat{p}_{\mathrm{sd}}$ could be misleading, because at these values, the channel is closed and the transistor is effectively off. For the device to be capable of amplifying the small-signal gate pressure, the channel should not be closed over the entire swing of the gate pressure. It should also be mentioned that the actual gain when the device is loaded is different from the unloaded gain given by Eq. (41). In particular, if the load is dissipative, with resistance R_L, the output resistance is effectively the

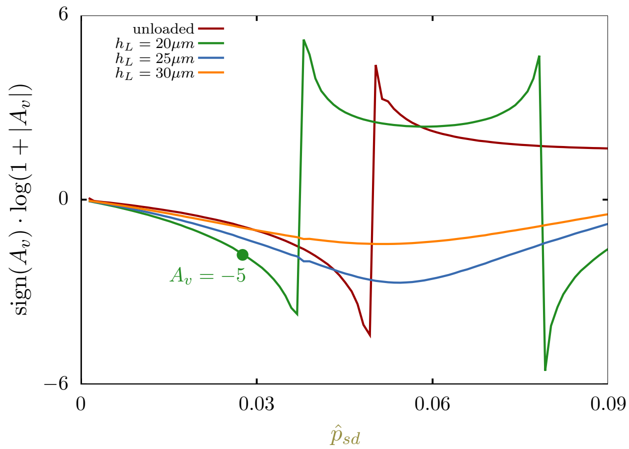


Fig. 18 Loaded gain of the (common-source) single-membrane microfluidic transistor. *Solid Lines* model. *Dashed lines* Ansys FSI

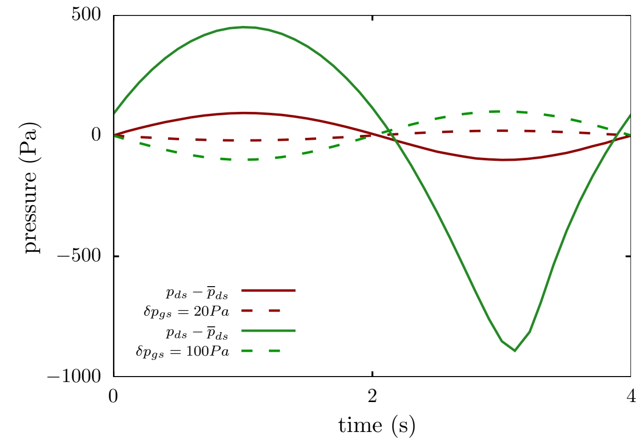


Fig. 19 Amplification of the common-source configuration of the single-membrane transistor for a harmonic pressure input at the gate for two values of δp_{gs}

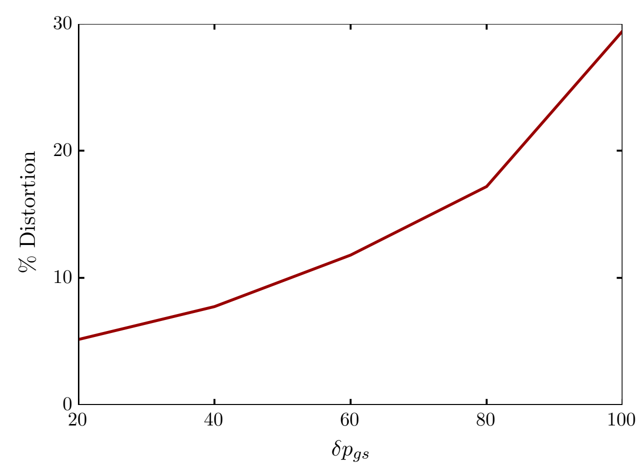


Fig. 20 Signal distortion versus input gate pressure signal amplitude, measured as $100\frac{||p'_{\text{ds}} - |A_v|p'_{\text{gs}}||}{||p'_{\text{ds}}||}$, $p'_{\text{ds}} = p_{\text{ds}} - \bar{p}_{\text{ds}}$, $p'_{\text{gs}} = p_{\text{gs}} - \bar{p}_{\text{gs}}$

small-signal output resistance in parallel with the load,[2] $r_o//R_L$, resulting in a loaded pressure gain of

$$A_v = g_m \frac{R_L r_o}{R_L + r_o}, \tag{48}$$

which reduces the gain if $r_o > 0$. If $0 < R_L << r_o$, the loaded gain can be approximated as $g_m R_L$. If, however, $r_o < 0$, which is the case for $\hat{p}_{\text{sd}} > \hat{p}^*_{\text{sd}}$, R_L can be chosen so that the effective output resistance $r_o//R_L$ is positive, negative, and even infinite is $R_L = -r_o$. The operating point should be chosen such that $r_o//R_L$ does not change over the entire gate–pressure and source–drain pressure swings. If the device is to be equipped with a feedback to realize an op-amp, then stability requires $r_o//R_L$ to positive. Figure 18 shows the variation in the loaded gain of the single-membrane transistor versus the source–drain pressure for $\hat{p}^*_{\text{gs}} = -0.0322$. The resistive load is realized by a 2D channel of length 1000 µm. The different curves correspond to different values of the channel height. For channel height larger than 25 µm, the load resistance is such that $R_L//r_o$ is positive over the entire range of the source–drain pressure.

The maximum source pressure ($p_{\text{s,max}}$) and the channel length (L) and height (h_0) are expected to play roles analogous to the maximum drain supply voltage[3] V_{DD}, channel width W, and dopant distribution in a MOSFET. These parameters characterize the power consumption and speed of the device, and as technology improves, both V_{DD} and W decrease, indicating faster and lower power transistors. The bias gate and drain pressures are selected, and the transistor is sized so that g_m and r_o yield the desired gain when the device is loaded. Ideally, this should be achieved while minimizing the power consumption and device size. The transconductance, g_m, and the intrinsic output resistance, r_o, of the transistor are obtained from the characteristic curves of the transistor.

To illustrate the design process of a common-source configuration, we choose the operating point shown in Fig. 14 and labeled "OP." This operating point is chosen to be at the maximum flow rate for $\hat{p}^*_{\text{gs}} = -0.0322$. The corresponding values of the incremental output resistance and transconductance are marked, respectively, in Figs. 15 and 16. The resistive load consists of a 2D channel of 1000 µm length and 20 µm height. The loaded device is biased such that

[2] For the common-source configuration shown in Fig. 13, the effective output resistance is $r_o//R_L//R_D$.

[3] Conventionally, the supply voltage is referred to as V_{DD} in microelectronic circuits because it drives the drain of a p-MOS device.

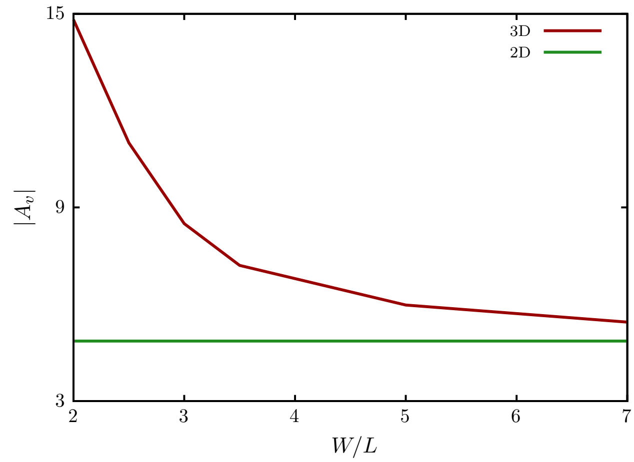


Fig. 21 Impact of the channel width on the unloaded gain

the gate–source and source–drain pressures match those of point "OP." This biasing requires the source–ground pressure to be 10,240 Pa. The loaded gain, as determined from the characteristic curves, is expected to be equal to -5, as shown in Fig. 18. A small-signal harmonic pressure is applied at the gate $p_{\text{gs}} = p_{\text{gs,DC}} + \delta p_{\text{gs}} \sin(2\pi f t)$, where $p_{\text{gs,DC}} = 1000$ Pa and the frequency f is chosen to be sufficiently small to avoid high-frequency effects caused by the source–gate and drain–gate capacitances. The time-varying component of the output pressure recorded at the drain, as computed from the transient Ansys FSI simulation, is plotted over one period in Fig. 19 for small-signal gate pressure of $\delta p_{\text{gs}} = 20$ and 100 Pa. It can be observed that for $\delta p_{\text{gs}} = 20$ Pa, the common-source configuration yields a gain equal to -4.9, as determined by the ratio of the peaks. This is expected since the input signal has a small amplitude so that the device behavior is linear. Note that the gain is negative, indicating that the output signal is inverted or 180° out of phase with respect to the input signal. As the amplitude of the input pressure signal at the gate is increased to 100 Pa, departure from the linear behavior is expected. If the departure is too large, the behavior may become unstable. This can be inferred from Fig. 18. If the amplitude of the input gate–source pressure is 100 Pa, the corresponding swing in the source–drain pressure (-449 to 891 Pa) will include the region where the gain switches from $-\infty$ to $+\infty$. One may conclude that realizing high gain is not useful if the output is unstable and/or distorted, as is the case with $\delta p_{\text{gs}} = 100$ Pa. Distortion of the output drain pressure, measuring the departure from a linearly amplified signal using an L_2 norm is shown in Fig. 20 to increase as the input gate pressure signal amplitude is increased.

4.4 Effect of finite channel width

The results presented so far were obtained from 2D simulations of the single-membrane transistor by using several assumptions to neglect the impact of the channel width on the fluid and solid mechanics. These assumptions are based on the observations that when the channel width is very large, the z-component of the stress in the membrane can be neglected and the effect of the side walls on the flow in the channel can also be neglected, thus allowing the device to be modeled as two-dimensional. In this section, we investigate the impact of the ratio of the channel width to channel length on the small-signal unloaded pressure gain, $\hat{A}_v$. In order to simulate the 3D problem, a 3D mesh of sufficient resolution is employed, and all the boundary conditions enforced in the 2D simulation are the same except that the membrane sides are replaced by fixed supports and the flow channel sides by no-slip walls. The results of the 3D and 2D simulations are compared to each other in Fig. 21, where the dependence of the $\hat{A}_v$ on W/L is shown. From the figure, it can be seen that the 3D gain converges to the 2D as W/L is increased. It is observed that higher gain is achieved as the aspect ratio of the channel cross section approaches unity. This may be attributed to two factors that contribute to increasing the incremental output resistance. The first is the larger stiffness of the membrane due to the additional fixed support that constrain its deflection into the channel as the flow pressure decreases due to the speeding up of the flow in the region where the gate deflection into the channel is largest. The second factor is attributed to the fact that the dependence of the flow rate on the channel height does not scale as h^3, which is valid for $W/h \to \infty$. In fact for $W/h = 1$, the flow rate scales as h^2. This implies that for a given deflection of the gate into the channel, the flow rate per unit width does not decrease as much compared with the 2D case.

As demonstrated previously, the single-membrane device is capable of realizing high gain over a narrow range of the source–drain pressure centered at $\hat{p}^*_{\text{sd}}$. Outside this range, the absolute value of r_o decreases which limits the gain. More importantly, this range of p_{sd} contains a singularity in the incremental output resistance and unloaded gain. This has significant impact on the stability and distortion. One way to increase the saturation range over which r_o is large and nonsingular is by using the dual-membrane transistor, introduced next. This allows for stable and less distorted output for larger input gate pressure signal amplitudes (swings).

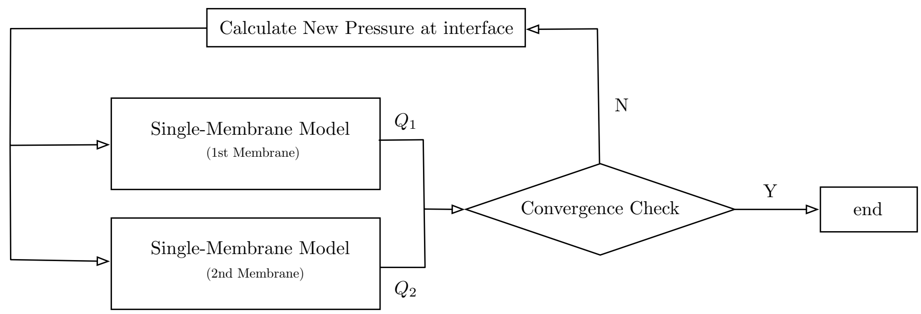


Fig. 22 Flowchart of the dual-membrane model implementation

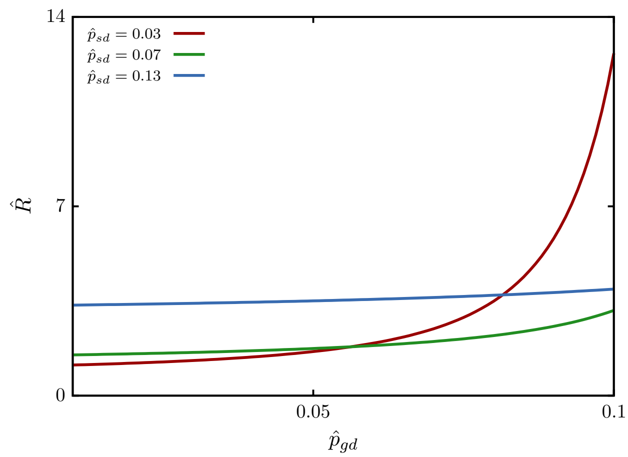


Fig. 23 Static (DC) resistance for the dual-membrane transistor

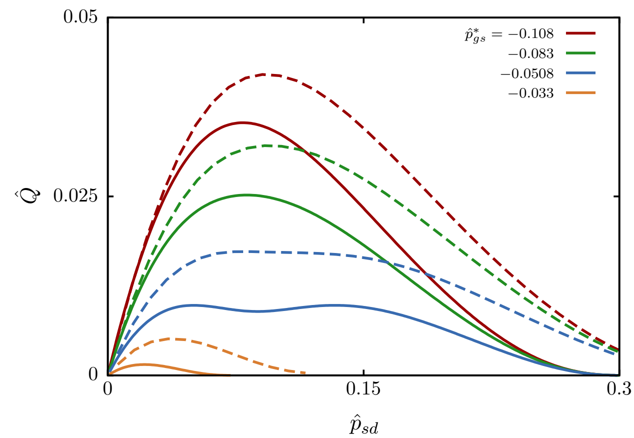


Fig. 24 Characteristic ($\hat{Q}-\hat{p}_{\mathrm{ds}}$) *curves* of the dual-membrane transistor. $\hat{Q}=Q/Q_{\mathrm{pois}}$ where $Q_{\mathrm{pois}}=\frac{wh_0^3p_0}{12\mu(L_1+L_2)}$. The gate pressure at which the channel closed is $p_g^*=10{,}800$ Pa. *Solid lines* reduced-order model. *Dashed lines* Ansys FSI

5 The dual-membrane transistor

In this section, we present the dual-membrane microfluidic transistor. This transistor consists of two elastic membranes next to each other with flow passing under them as shown in Fig. 2b. Both membranes have their edges fixed, with an external pressure ($\hat{p}_{\mathrm{g}}$) applied on the first membrane (gate), and the input (source) pressure ($\hat{p}_{\mathrm{s}}$) applied on the second membrane. The source–drain pressure difference ($\hat{p}_{\mathrm{sd}}=\hat{p}_{\mathrm{s}}-\hat{p}_{\mathrm{d}}$) is the sum of the pressure drops in the flow on the flow side of the membranes along the channel. The flow rate passing through the channel of the dual-membrane transistor is thus controlled by the combined effect of the pressure drop along the channel, $\hat{p}_{\mathrm{sd}}$, and the deflection of the two membranes. The deflection of each membrane is, in turn, controlled by the difference between the external pressure and the flow pressure in the channel. The motivation behind the dual-membrane transistor is to have an additional degree of freedom to enable us to adjust the $\hat{Q}-\hat{p}_{\mathrm{sd}}$ curve to have a larger range of $\hat{p}_{\mathrm{sd}}$ in which the device is in saturation (large $\hat{r}_o$ free of singularities).

Characterization of the various operating regions of the dual-membrane transistor is carried out in manner similar to that done for the single-membrane transistor. The static behavior of the device is discussed first, followed by a discussion of the small-signal behavior through the characteristic curves. The results are presented for a dual-membrane transistor with the following dimensions: The membrane lengths are $L_1=L_2=2470\,\mu$m, the thicknesses are $d_1=d_2=196\,\mu$m, the undeformed height of the channel is $h_0=59\,\mu$m, and the length of the entry channel is $L_z=500\,\mu$m. The reduced-order model of the dual-membrane transistor consists of two single-membrane channels connected in series, where the external pressure on the second membrane is equal to the input pressure of the first channel, in accordance with Fig. 2b. A flowchart is presented in Fig. 22.

5.1 Operating point (DC) characteristic curves

At static conditions, the dual-membrane device operates as a variable resistor controlled by the source–drain and gate–drain pressure differences, with the resistance given by Eq. (29). As observed in Fig. 23, the DC resistance dependence on $\hat{p}_{\mathrm{gd}}$ is similar to the single-membrane transistor for small values of $\hat{p}_{\mathrm{sd}}$. This dependence weakens as the source–drain pressure increases, as the second membrane

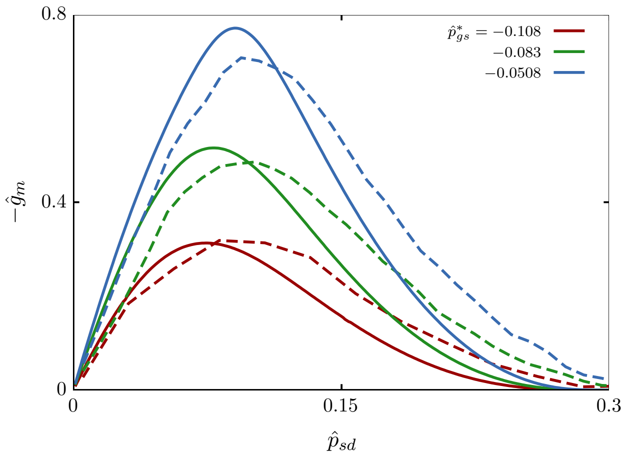


Fig. 25 Transconductance of the dual-membrane transistor. *Solid lines* reduced-order model. *Dashed lines* Ansys FSI

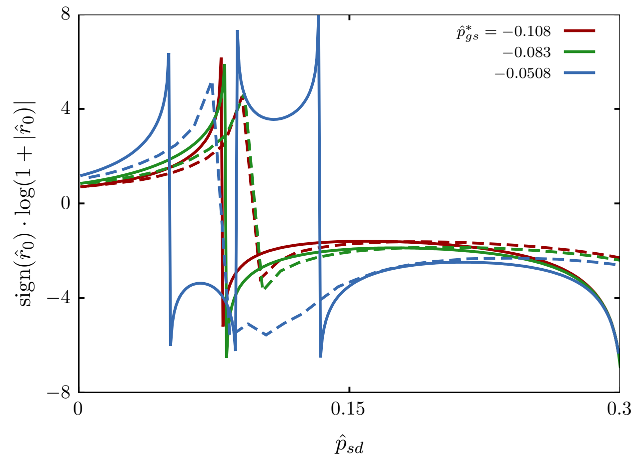


Fig. 26 Intrinsic output resistance of the dual-membrane transistor. *Solid lines* reduced-order model. *Dashed lines* Ansys FSI

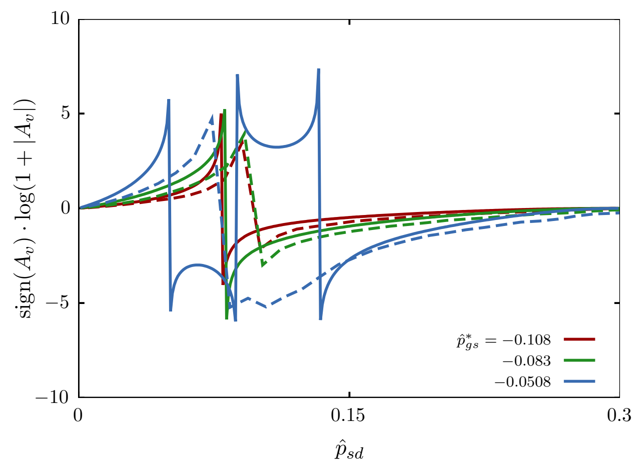


Fig. 27 Gain (unloaded) of the dual-membrane transistor. *Solid lines* reduced-order model. *Dashed lines* Ansys FSI

starts to close the channel. This behavior is due to the fact that increasing the source pressure causes an increase in the channel height along the first membrane and a decrease in the channel height along the second membrane. In this case, the resistance to the flow is dominated by the deflection of the second membrane and is weakly dependent on the gate pressure over the presented range of $\hat{p}_{gd}$. For $\hat{p}_{sd} << \hat{p}_{gd}$, the high pressure at the gate causes the first membrane to deflect toward the channel, thus dominating and controlling the resistance to the flow.

Dependence of the source–drain flow rate, $\hat{Q}$, on the source–drain pressure, $\hat{p}_{sd}$, for different values of the gate–source pressure, $\hat{p}^*_{gs}$, is plotted in Fig. 24 for the dual-membrane transistor. Upon inspecting the figure, the following operating regions can be identified: (1) linear rising regime, (2) saturation region, and (3) linear falling regime terminated with shutdown. At low values of the source–drain pressure, the device is in the linear region, and it operates as a resistor controlled by the gate–source pressure difference. When the source pressure approaches $\hat{p}^*_{sd}$, at which the flow rate is maximum, the device enters the saturation region where the flow rate starts to saturate. Increasing the source–drain pressure even more will cause the device to enter another linear regime where an increase in the source–drain pressure causes a decrease in the flow rate. What differs from the single-membrane behavior is that the saturation region is observed to extend over a larger range of the source–drain pressure over a range of gate–source pressure. In particular, when $\hat{p}^*_{gs} = -0.0508$, the saturation region predicted by Ansys FSI simulation extends from $\hat{p}_{sd} = 0.08$ to 0.15. This behavior, not present in the single-membrane transistor, is caused by the deflection of the second membrane toward the channel at high values of the source pressure. Similar regions are observed in the electronic MOSFET, but the saturation region in a typical MOSFET is wider than that of the dual-membrane microfluidic transistor presented in Fig. 24.

5.2 Small-signal parameters

The small-signal behavior of the dual-membrane microfluidic transistor is characterized by plotting the intrinsic output resistance, the transconductance, and the small-signal pressure gain against $\hat{p}_{ds}$ in Figs. 25, 26, and 27, respectively, for different values of $\hat{p}_{gs}$.

It can be seen from Fig. 25 that the maximum transconductance is realized somewhere between the linear region and the saturation region. As for the intrinsic output resistance, it reaches its maximum in the saturation region where the flow rate is maximum, since the intrinsic resistance is

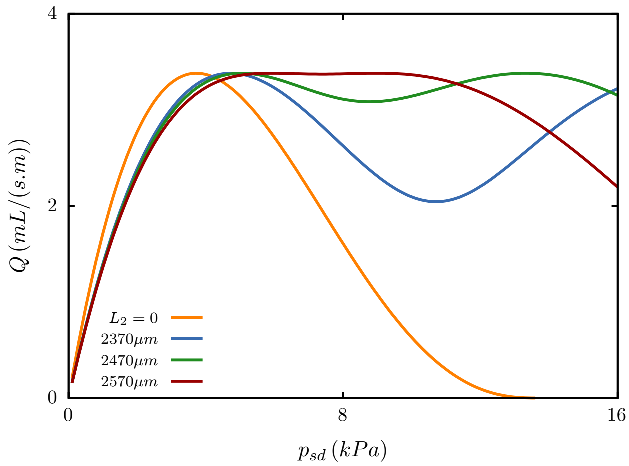


Fig. 28 Impact of changing the length of the second membrane on the dependence of the flow rate on the source–drain pressure difference

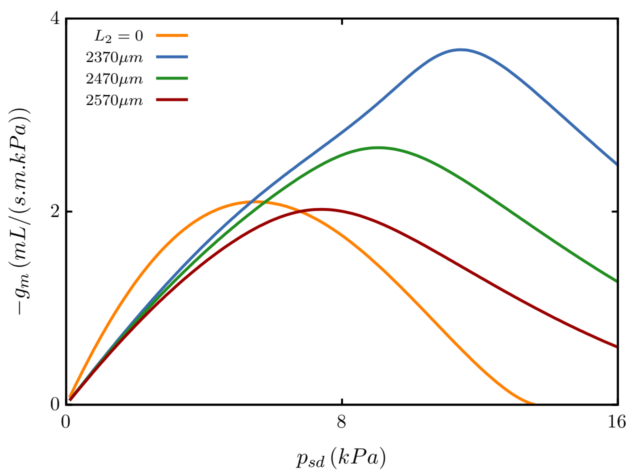


Fig. 29 Impact of modifying the length of the second membrane on the dependence of the transconductance on the source–drain pressure difference

the inverse of the slope of the $Q - \hat{p}_{\rm ds}$ curve for a given $\hat{p}_{\rm gs}$. These trends of $\hat{g}_m$ and $\hat{r}_o$ produce the unloaded small-signal pressure gain (Eq. 41) shown in Fig. 27. The small-signal gain A_v attains its peak values for large values of $\hat{r}_o$, where the device is in the saturation region. By observing Figs. 25 and 26, it can be seen that the dual-membrane transistor succeeded in achieving higher gains than its single-membrane counterpart. This is due to its ability to partially decouple the transconductance from the intrinsic output resistance, thus allowing it to maintain higher transconductance levels in the saturation region, where the incremental output resistance is large.

As mentioned previously, when the device is loaded at the drain, the output resistance is effectively the

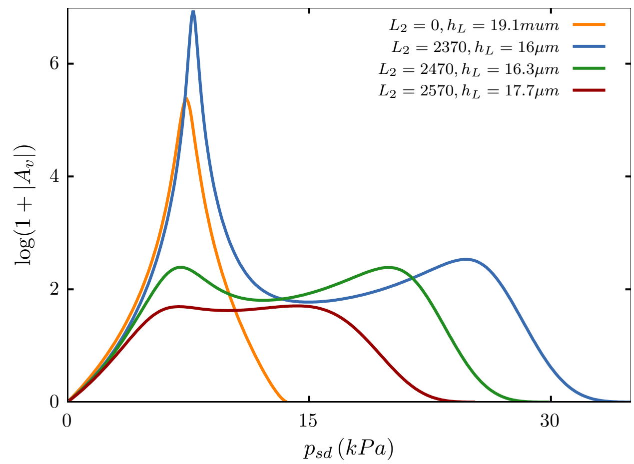


Fig. 30 Impact of changing the length of the second membrane on the dependence of the loaded gain on the source–drain pressure difference. The load is a 2D channel of length 1000 µm and height h_L. $L_1 = 2470$, $p_{\rm gs} = 5000$ Pa, $p_{closing} = 10{,}00$ Pa, $p^*_{\rm gs} = -0.0581$, $h_0 = 59$ µm, $d = 196$ µm

small-signal output resistance in parallel with the load resistance, resulting in a loaded small-signal pressure gain given by Eq. (48). One can see from (Eq. 48) that for a given R_L, the operating point that yields the highest loaded gain is generally not the same as the operating point of the highest unloaded gain, except when $R_L/r_o \to \infty$. In particular, when $R_L/r_o \to 0$, the loaded pressure gain becomes equal to $g_m R_L$ and in this case, the ratio of the loaded to the unloaded gain is R_L/r_o.

5.3 Controlling the saturation region

In this section, we investigate the impact of changing the length of the second membrane, L_2, on the $\hat{Q} - \hat{p}_{\rm ds}$ characteristic curves, the transconductance, and on the loaded gain, as predicted by the model. Figure 28 shows how increasing the length of the second membrane impacts the dependence of the flow rate on the source–drain pressure, for a gate–source pressure of $p_{\rm gs} = 5000$ Pa. Increasing L_2 from 0 (i.e., single-membrane device) to 2470 µm expanded the saturation region significantly.

The corresponding impact on the transconductance is shown in Fig. 29, where increasing the length of the second membrane is accompanied by an increase in the transconductance that shifts to higher source–drain pressures (as L_2 increases from 0 to 2370 µm), followed by a decrease that shifts to the left (as L_2 increases from 2370 to 2570 µm). The resulting loaded gain is shown in Fig. 30, where the dual membrane clearly outperforms the single-membrane device in terms of linearity and the size of source–drain pressure range over which the loaded gain is large. Note that the load for each device is chosen to be large enough

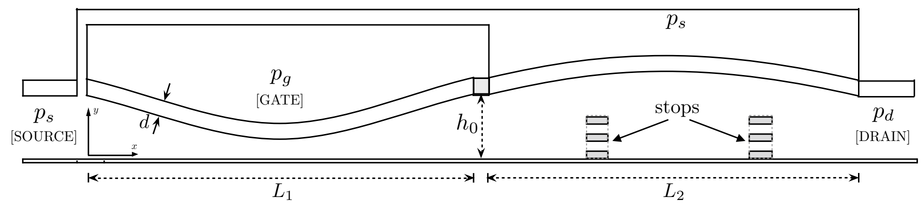


Fig. 31 Dual-membrane transistor with stops

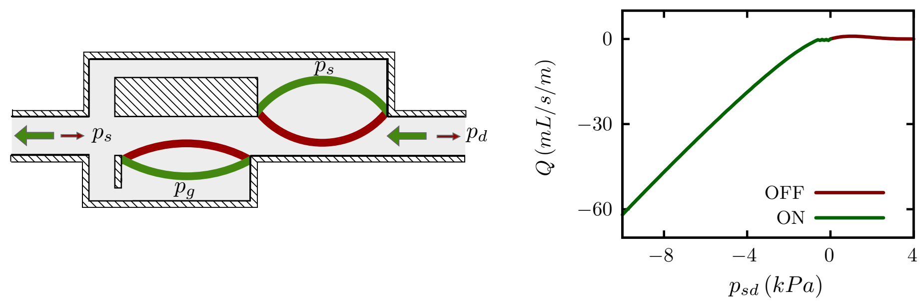


Fig. 32 Diode configuration of the dual-membrane microfluidic transistor

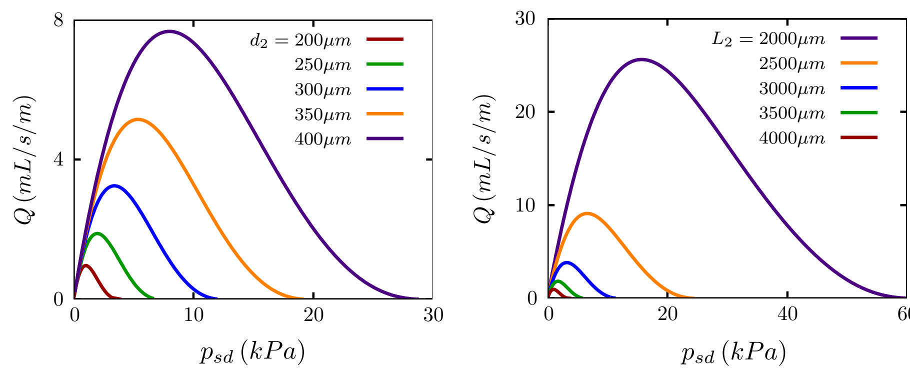


Fig. 33 Modifying the source–drain pressure at which the channel closes for diode operation

so that the gain does not switch sign over the entire source–drain pressure range.

The linear falling regime, characterized by closing the channel at a sufficiently high value of the source pressure, can be eliminated or modified by placing stops in the channel beneath the second membrane, thus constraining its deflection, as depicted in Fig. 31. Placing these stops that have perforations that allow the flow to pass through is expected to further widen the range of the source–drain pressure over the saturation region.

6 Applications

The single-membrane transistor can be used as a switch (valve) controlled by the gate pressure or as a digital amplifier for microfluidic logic control, as mentioned in the introduction. In logic circuits, the transistor is driven with a gate voltage of large swing so that the device switch from on to off (or off to on) with the output pressure at the drain operating between its maximum and minimum (rail to rail). In this case, stability and distortion are not critical issues as long as the device does not fail. The relaxation of these restrictions allows choosing operating points where the gain is large.

In this section, we explore some of the applications of the dual-membrane microfluidic transistor.

6.1 Diode and safety shutdown

The dual-membrane device can be used a diode that is self-actuated, which differs from the valve controlled by the gate pressure. Operation of the diode is shown in Fig. 32(left). Note that in the diode configuration, the gate is connected to the source. If the source pressure is larger than the drain pressure, the second membrane starts closing. The value of the source–drain pressure at which the channel closed, $p_{\mathrm{ds,th}}$, can be decreased/increased by increasing/decreasing the compliance of the second membrane. Impact of increasing the compliance of the second membrane by increasing its thickness is shown in Fig. 33(left).

Reducing the second membrane thickness from 400 to 200 µm increases its compliance and lowers $p_{\mathrm{ds,th}}$ from 30

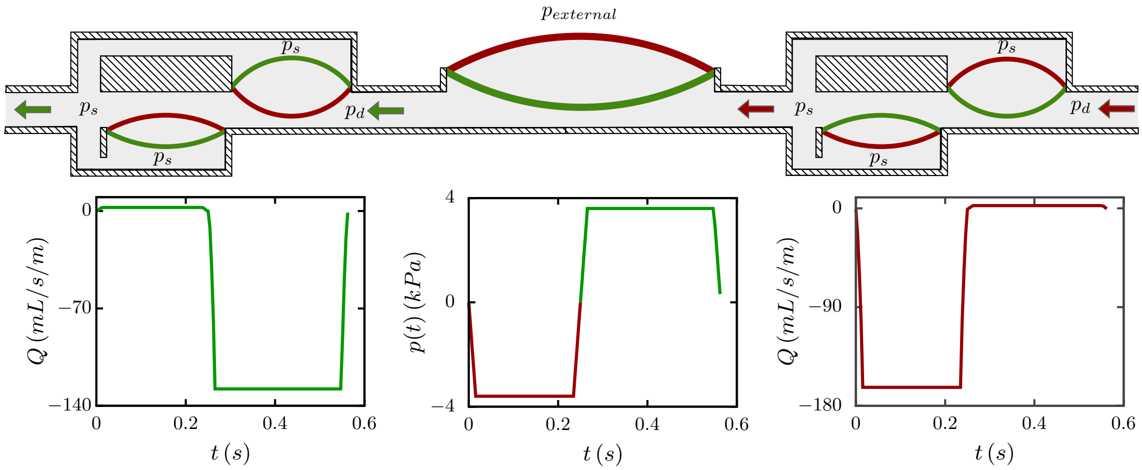


Fig. 34 Employing the diode configuration of the dual-membrane device in the operation of a micropump

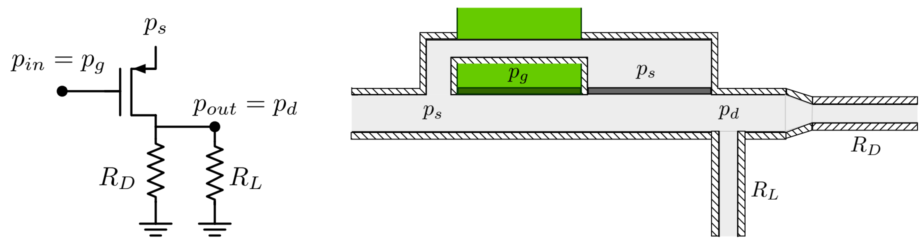


Fig. 35 Dual-membrane device in a common-source configuration

to 3 kPa. Figure 33(right) shows the impact of increasing the second membrane length on $p_{\mathrm{ds,th}}$. If the drain pressure is larger than the source pressure (i.e., if $p_{\mathrm{ds}} < -p_{\mathrm{ds,th}}$), both membranes are deflected away from the channel and the flow pass through, which is captured by the performance curve shown in Fig. 32(left). Note that for larger value of d_2, the device operates as a shutdown switch, which stops the flow if the pressure amplitude becomes too large.

An example application employing the device as a diode device is the operation of the micropump depicted in Fig. 34. When the external pressure decreases in the first half of the cycle (lower-middle plot), the diode on the left closes and the one on the right opens so that the flow entering from the right fills the chamber. In the second half of the cycle, the external pressure is increased pushing the pump membrane inward forcing the fluid to leave through the left diode, which is open. During this half cycle, the diode on the right is closed. The flow rates through the left and right diodes over one operation cycle are shown in the lower left and right plots of Fig. 34.

Other applications of the diode-connected device include (1) signal rectification, (2) signal limiting and regulation, (3) current mirroring where the device is used to copy a reference flow rate, and (4) in differential amplifier pairs, which are attractive because they lower the distortion

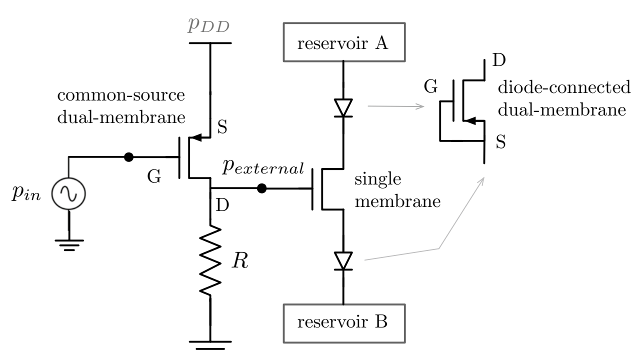


Fig. 36 Using a common-source (dual-membrane) amplifier to drive the gate of a single-membrane device operating as a pump equipped with two diodes

by removing the second harmonics. These applications will be the subject of future work.

6.2 Common-source amplifier

The dual-membrane microfluidic transistor employed in a common-source amplifier configuration is shown in Fig. 35(right) along with its electronic counterpart (left). We consider two applications of the common-source amplifier: (1) the common source driving the membrane of the

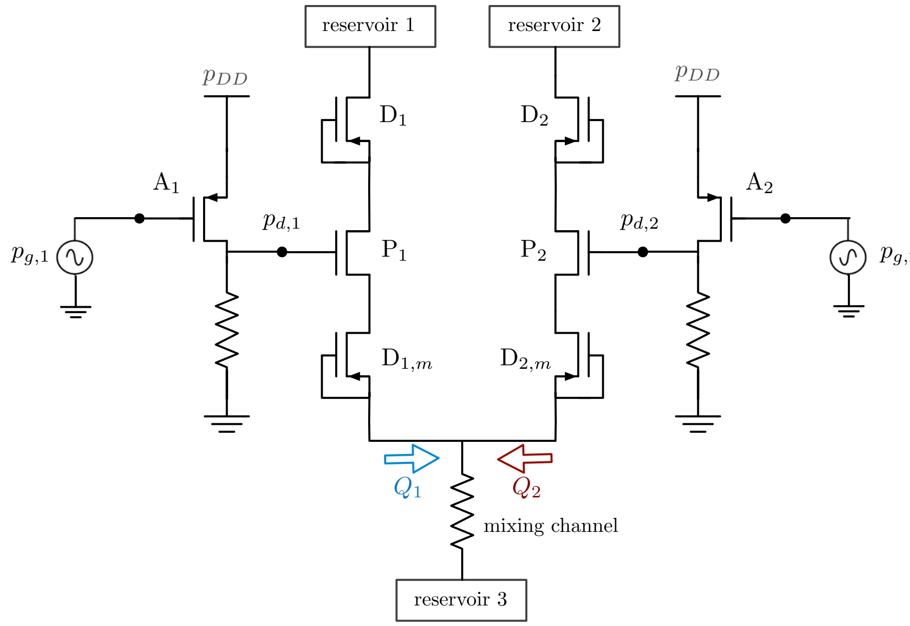


Fig. 37 Employing the common-source amplifier in a mixing circuit using pulsating flows

micropump shown in Fig. 34, and (2) using the pump for mixing of biological species using two pulsating microfluidic streams.

6.2.1 *Common source driving a micropump*

The external pressure applied to the membrane of the pump shown in Fig. 34 can be realized as the output of a common-source amplifier, as depicted in Fig. 36. In this case, the amplified signal at the drain of the common source, $p_{\text{external}} = p_{\text{ex,DC}} + A_v p_{\text{in}}$, can be used to actuate the gate of a single-membrane transistor. The DC pressure, $p_{\text{ex,DC}}$, is the bias pressure of the drain of the common source and is equal to $Q_{\text{bias}}R$, where Q_{bias} is the bias DC flow rate from source to drain. The resistance R can be realized using a channel or using a diode-connected transistor. Using a diode-connected transistor instead of a resistor increases the gain since it increases the output impedance. Since the common source is driving the gate of a single-membrane device, the input impedance looking into the gate of the single-membrane device is capacitive. Since the impedance looking into the gate of the single-membrane device is capacitive, high gains can be realized since the resistive part of that impedance is infinite.

6.3 Micromixing

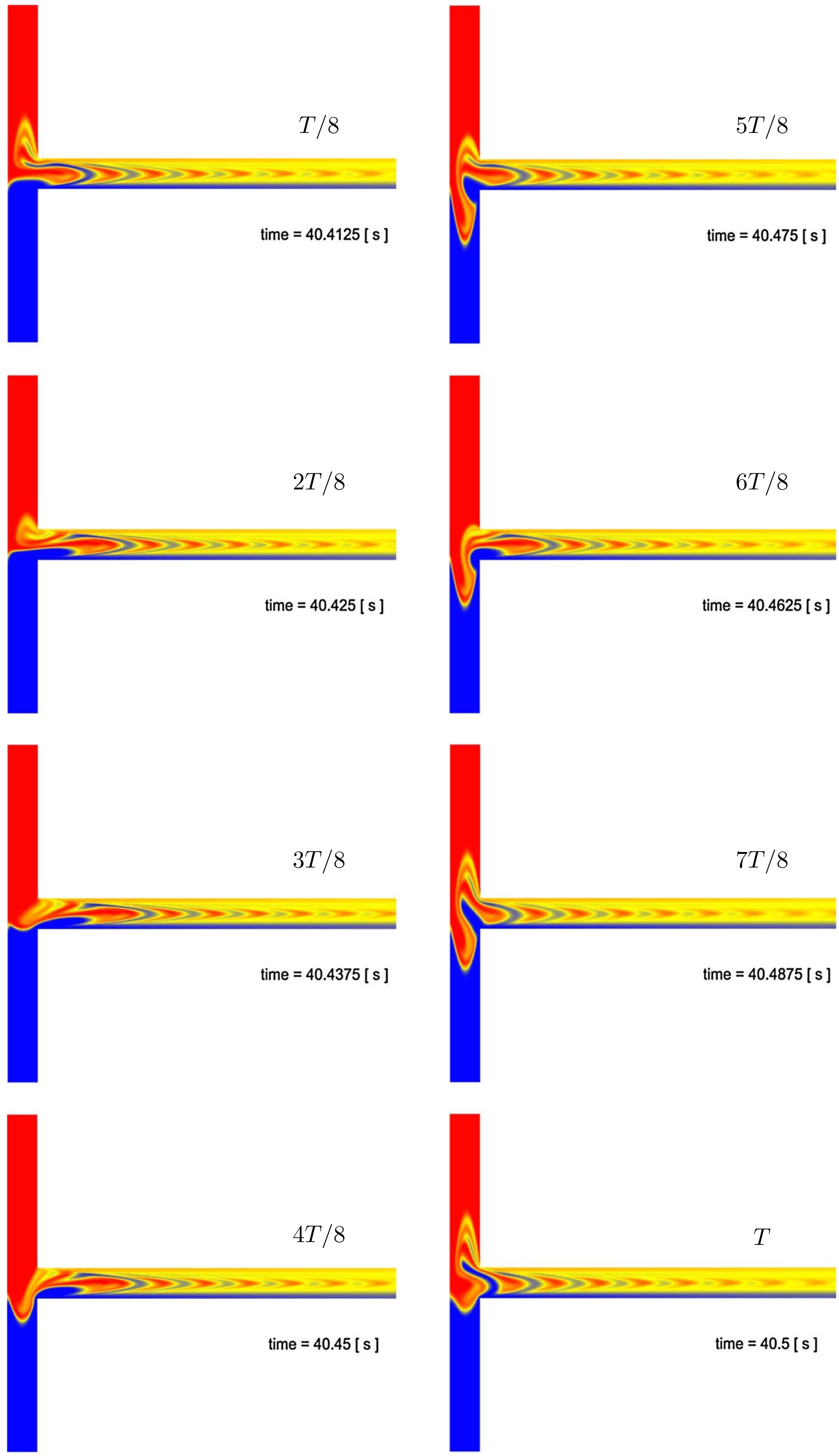
The common source amplifier driving a micropump in Fig. 36 can be used for mixing of biological or chemical species using pulsating flows. Mixing on the microscale is challenging due to the fact that these species typically have a small mass diffusion coefficient, which, in the absence of turbulence, limits the mixing process. A schematic of the proposed mixing circuit is presented in Fig. 37.

The two pulsating flows take place in the channels connected to mixing channel, as shown in Fig. 37. Both common-source amplifiers have the same supply total pressure p_{DD} at the source. The pressures applied at the gates of the common-source transistors have the form $p_{\text{g},1} = p_{\text{g},0} + \delta p_{\text{g}} \sin(2\pi ft)$ and $p_{\text{g},2} = p_{\text{g},0} + \delta p_{\text{g}} \sin(2\pi ft + \phi)$, where ϕ is the phase difference. The common-source amplifiers will amplify the time-varying component of the gate pressure and produce output (drain) pressures of the form $p_{\text{d},1} = p_{\text{g},0} + A_v \delta p_{\text{g}} \sin(2\pi ft)$ and $p_{\text{d},2} = p_{\text{d},0} + A_v \delta p_{\text{g}} \sin(2\pi ft + \phi')$, assuming the amplification is linear. These drain pressures will create two, out of phase, pulsating pressures actuating the gates of the pumps. The diodes D_1 and D_2 ensure that the flow is established from reservoirs 1 and 2 into the pump but not in the opposite direction. Diodes, $D_{1,m}$ and $D_{2,m}$, connecting the pump to the mixing channel are designed to allow flow in the reverse direction so that at the branches leading to the mixing channel, the following flow rates are realized: $Q_1 = Q_0 + \delta Q \sin(2\pi ft)$ and $Q_2 = Q_0 + \delta Q \sin(2\pi ft + \phi')$, where ϕ' is the phase difference between the two flows.

Efficient mixing using pulsating flows (Glasgow et al. 2004) has been reported for $\delta Q/Q_0 > 1$ and $\phi' = \pi/2$ and at an optimal pulsating frequency $f_{\text{opt}} \sim \delta V/D_h$ above and below which the mixing efficiency deteriorates (Cheaib et al. 2015).

Driving the gate with pressure signals at a frequency of 10 Hz and with a 90° phase difference and designing the common-source amplifiers, pump, and diodes so

Fig. 38 Degree of mixing at different stages of the pulsation period



that $\delta Q/Q_0 = 10$ produce the mixing behavior shown in Fig. 38. In the figure, the degree of mixing is shown at different time steps with respect to the period T. As shown, mixing between the two flows entering the mixing channel is well established throughout the channel.

It should finally be noted that the circuit presented is not the only way mixing using pulsating flows can be realized. Mixing may also be realized using the microfluidic oscillator presented in Mosadegh (2010) or the device presented in Leslie et al. (2009), where flow-switching between the two reservoirs is achieved by combining two frequency-selective branches. In Glasgow et al. (2004), an external peristaltic pump is employed. The authors in Glasgow et al. (2004) suggested that future designs could generate pulsing by electrostatic actuation of integrated diaphragms or even externally actuated elastomeric PDMS membranes incorporated in the device.

7 Conclusion

Two microfluidic transistors that employ the elastic membrane microchannel channel are presented.

Reduced-order models that capture the low-inertia dynamic behavior of the coupled fluid–solid problem were developed to enable fast small-signal analysis of large circuits. The models, when compared to detailed numerical simulations of the coupled fluid–structure interaction problem over a wide range of operating pressures, proved to be most accurate when the inertia of the flow in the channel is small.

Characterization of the analog behavior of the two devices is expressed in terms of dependence of the volume flow rate versus the source–drain and gate–source pressure differences, analogous to the characteristic curves of MOSFET operation. The characteristic curves are then used to extract the small-signal parameters (transconductance and intrinsic output resistance), characterizing the dynamic response to small time-varying pressures at the gate and/or drain.

For the single-membrane device, the characterization revealed that, depending on these operating pressure differences, the device operates as a capacitor when the membrane is deflected away from the channel and as a transistor when it is deflected into the channel. When the flow inertia is sufficiently high, a negative capacitive behavior is observed at high gate pressures. In the transistor regime of operation, the device is capable of providing large gains. Due to the narrowness of the saturation regime, the linearity is poor and distortion is high.

The dual-membrane transistor proposed is shown to improve linearity and reduce distortion by expanding the saturation zone. In addition to its operation as a transistor, the dual-membrane design is also shown to operate as a diode and a shutdown safety switch.

Finally, the dual-membrane transistor is used to drive a micropump equipped with two diodes. The micropump is then employed in a larger circuit that performs mixing of two species using pulsating flows.

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