CAMEM: A Computationally-Efficient and Accurate Memristive Model With Experimental Verification

Basma Hajri, Mohammad M. Mansour, *Senior Member, IEEE*, Ali Chehab, *Senior Member, IEEE*, and Hassen Aziza

Abstract—**When using memristive devices at the circuit level, a simple, accurate, and computationally efficient model is critically required to predict the performance of the circuit. Various memristive device models have been developed in the literature; however, most of them suffer from high complexity, low accuracy, or low computational efficiency. In this paper, a novel model for memristive devices for use at the circuit level is proposed. The proposed model is compact, sufficiently simple, computationally efficient, and compatible with popular circuit simulators. Moreover, the model meets circuit designers' requirements in terms of accuracy to explore new memristor-based design architectures. An experimental validation of the model is also provided.**

Index Terms—**Memristive models, compact model, resistive random access memory (RRAM), experimental validation.**

I. Introduction

Known for their excellent performance, good scalability, and quick programming, Resistive Random-Access Memory (RRAM) devices have recently acquired massive attention. A primary form of RRAM component is a Metal/Insulator/Metal (MIM) structure, referred to as a memristor, acting as a variable resistor that can "remember" the last charge that was flowing through it. For circuit-level simulations, an essential requirement when using memristive devices is an accurate and designer-friendly model to guide users throughout the design process. To enhance the understanding of the memristive behavior, and also use its particular characteristics at the system level in different applications, an accurate physical model of the memristive device should be developed. However, commonly, such models are complex and computationally inefficient.

A version with simple expressions instead of the complicated equations is then highly desired. However, the simple model should maintain adequate accuracy.

Typically, tools used to simulate large scale memristor arrays can handle up to 3,000 memristive devices, and after that, the simulation runtime becomes enormous [1]. Since these tools are non-parallel simulators (i.e., a single-core processor), performing simulations of large-scale memristor crossbar architectures can sometimes take over 3 days [2].

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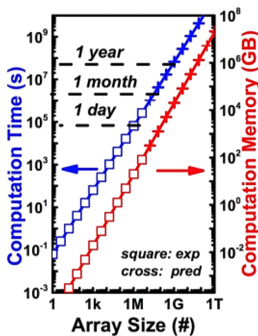

Fig. 1. Array size impact on computation time and computation memory [4].

This work aims to provide memristor users with an accurate physical model with simpler equations, and which is computationally efficient.

The manuscript is organized into six sections. Section II gives an overview of the popular memristor complex models. Section III introduces the proposed model equations and parameters. Section IV shows the simulation results and a fitting of the proposed model to a reference model. Section V presents an experimental validation of the model. Finally, Section VI is the summary of the paper.

II. Overview of Memristor Complex Models

Lately, memristor research has received increasing attention in different applications, including resistive memories, analog/digital circuits, computers, neuromorphic design, sensors …[3]. Therefore, to effectively use memristors in different applications, it is required to develop appropriate memristor models that can be easily used throughout the design process. To correctly catch the fundamental memristor device properties for simulations, physics-based device models are commonly used. Nonetheless, using such models for simulations of large memristor arrays remains impossible because of the considerable computing resources required. As shown in Fig. 1, to simulate a 400 Mb memristor array, it may take about a year [4].

If the memristive model equations use exponents and hyperbolic functions and not polynomials, the model is considered complex [5]. Despite the computational inefficiency, exponential and hyperbolic sine functions are used in several memristor

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models in the literature. Hyperbolic sine function is typically used in physics-based device models since it shows a good representation of the memristor hysteresis. Schottky barrier created between the oxide layer and the memristor bottom electrode is accurately defined by exponential functions [6]. This detailed representation of the I–V characteristic is required in all memory applications, for instance. However, in other applications like neuromorphic computing or logic-in-memory, using a model capturing only the resistance characteristic is highly efficient for large scale arrays [7].

In this study, we focus on the following physics-based complex models: the non-Linear Ion Drift Model [8], the Simmons Tunnel Barrier Model [9], and the Stanford model [10]. We selected these models since they represent different types of physics-based complex equations used in general to model the memristive devices.

A. Non-Linear Ion Drift Model

This model is an improvement of the linear ion drift model proposed in [8]. It assumes a nonlinear relationship between the voltage and the internal state derivative. This memristor model is mainly used in logic circuits. The current equation is defined as follows:

$$i\left(t\right) = \omega(t)^{n}\beta \sinh\left(\alpha v\left(t\right)\right) + \chi\left[\exp\left(\gamma v\left(t\right)\right) - 1\right] \quad (1)$$

$\beta, \chi,$ and γ are experimentally extracted parameters; $\omega \in [0, 1]$ is the state variable parameter, *n* is a parameter that defines how the state variable affects the current. The switching behavior of the memristor device, in this model, is assumed asymmetric. When the memristor has a low resistance state (ON), ω is around 1, and the hyperbolic function of (1) (i.e., $\beta \sinh(\alpha v(t))$) dominates the current equation, this defines the tunneling phenomenon. When the memristor has a high resistance state (OFF), ω is around 0, and the current equation is dominated by the second term (i.e. $\chi[\exp(\gamma v(t)) - 1]$); thus, (1) is similar to the equation of an ideal diode. The differential equation of the state variable is:

$$\frac{d\omega}{dt} = a \cdot f\left(\omega\right) \cdot v(t)^{m} \quad (2)$$

$f(\omega)$ is a window function, *a* and *m* are two constants, and *m* is an odd integer.

B. Simmons Tunnel Barrier Model

An advanced physical memristor model with higher accuracy has been developed in [9]. The physical structure, assumed in this model, is an electron tunnel barrier in series with a resistor instead of two series resistors as in the first HP model. The memristor switching behavior, in this model, is assumed asymmetric and non-linear. An implicit equation (3) defines the current-voltage dependence where A is the channel area of the memristor, e is the electron charge, vg is the voltage across the tunnel barrier, m is the mass of the electron, h is Planck's constant, and ϕ_{I} is the barrier height in electron volts.

$$i = \frac{e\mathrm{A}}{2\pi h \Delta\omega^{2}}\left\{\phi \mathrm{I} e^{-\mathrm{B}\sqrt{\phi \mathrm{I}}} - \left(\phi \mathrm{I} + \mathrm{e}\left|\mathrm{vg}\right|\right) e^{-\mathrm{B}\sqrt{\phi \mathrm{I} + \mathrm{e}\left|\mathrm{vg}\right|}}\right\}$$
$$B = \frac{4\pi\Delta\omega\sqrt{2\mathrm{m}}}{h} \quad (3)$$

$$\frac{dx\left(t\right)}{dt} = \begin{cases} c_{off}\sinh\left(\frac{i}{i_{off}}\right)\exp\left[-\exp\left(\frac{x-a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right], & i > 0 \\ c_{on}\sinh\left(\frac{i}{i_{on}}\right)\exp\left[-\exp\left(-\frac{x-a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right], & i < 0 \end{cases} \quad (4)$$

The state variable x represents the Simmons tunnel barrier width. Hence, $\frac{dx(t)}{dt}$ can be considered as the velocity of oxygen vacancy drift shown in (4). The parameters c_{off}, c_{on}, i_{off}, i_{on}, a_{off}, a_{on}, w_c, and b are fitting parameters, R_s is the channel resistance, *v* is the internal voltage of the device, and V_g is the voltage of the oxide region.

C. Stanford Model

This model is compact and accurately depicts the bipolar switching characteristics of metal oxide resistive memory elements [10]. The current in the RRAM cell is given by:

$$I = I_0 \exp\left(-\frac{g}{g_0}\right)\sinh\left(\frac{V}{V_0}\right) \quad (5)$$

In this equation, *V* is cell voltage; the voltage coefficient V_0, the gap coefficient g_0, and the pre-factor I_0 are two parameters extracted experimentally. The distance separating the metal electrode from the edge of the conductive filament is g which is Hence, the main variable defining the RRAM cell resistance. The gap distance evolution rate induced by the filament growth/rupture follows an exponential law [10]. It is calculated while considering the electric field, the migration of oxygen ion, and the Joule heat local temperature. Furthermore, the model includes the stochastic and temperature-dependent filament movement (δg).

D. Other SPICE Models

Several SPICE models have been proposed to overcome the complexity and limited computational efficiency of [8], [9].

The ThrEshold Adaptive Memristor model (TEAM) [11] uses the physics principle proposed in [9] but with more straightforward mathematical equations. In this model, the state variable does not change unless the applied current exceeds a certain threshold. Moreover, the equations relating the current to the internal state derivative use polynomials rather than exponentials. The computational efficiency of the TEAM model is higher than the Simmons tunnel barrier model.

A modified version of the TEAM model is proposed in [12] using a threshold voltage rather than a threshold current. This model is appropriate for certain logic and memory applications. Another SPICE model that exhibits voltage threshold is developed in [13]. This model appears to match well the characterization data of different memristors.

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New SPICE models with simpler analytical approximations have been developed to overcome the complexity of the memristor physical processes mathematical implementation. Bayat *et al*. proposed a TiO2 memristor SPICE model based on Simmons Tunnel Barrier Model, but with improved accuracy and lower numerical simulation cost [14]. However, in this model, only mathematical approximations of measured characteristics are used with no qualitative insight.

Alternatively, several behavioral models (e.g., those by Biolek [15], [16]) simplify the physical memristor mechanism to some useful abstractions fitted to the experimentally observed behaviors to maximize the size of the memristive networks.

E. Models Comparison

Most of the accurate physical models of memristors, proposed in the literature, present a considerable computational efficiency problem in large-scale memristor arrays, which can introduce convergence issues [17]. Problems of solution-accuracy caused by the improper numerical integration of the equations in most complex models have been appropriately addressed in [18], and techniques to improve the convergence are also developed. However, the computational efficiency and convergence issues persist for very-large-scale memristor arrays. The concept of threshold in memristor switching is a main characteristic demonstrated experimentally on most of actual memristor devices. Physical memristive devices commonly show a voltage limit where hysteresis is not generated until the memristor applied voltage surpasses this limit known as threshold [19]. Several models listed in this section [10]–[15] include the threshold effect. However, several memristors show different threshold values during SET and RESET phases, depending on the polarity of the applied voltage [12], [13]. Another substantial effect that should be included in a memristor model is the device variation that may affect the performance at the circuit level. Only models [10] and [13] provide this effect. Furthermore, most of the existing physics-based complex models suffer from being ill-posed [20] and mainly suffer from division-by-zero errors and DC response problems.

The motivation of this paper is to propose a memristor model that captures well the memristor physics and overcomes all the limitations mentioned above.

III. Computationally Efficient and Accurate Memristive (CAMEM) Model

A novel model with simpler expressions is therefore proposed to overcome the limitations mentioned above while maintaining adequate accuracy. This simplified model includes the central part of the memristor dynamics reproduced by more complex models, but with simpler mathematical functions to ensure simple analysis, easy understanding, and computational efficiency. The model has been implemented in Verilog-A and is SPICE compatible. The following approximations are used in the model; a global state variable w_p (corresponding to conductive filament growth), different threshold voltages (V_{TS} and V_{TR}) for both SET and RESET phases are introduced, different initial condition currents (I_{0S} and I_{0R}) corresponding to the hopping current density in the filament region during SET/RESET phases, and polynomial dependence rather than hyperbolic functions is used.

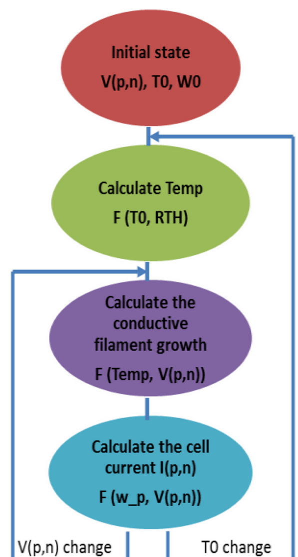

Fig. 2. General flowchart of the CAMEM model implementation.

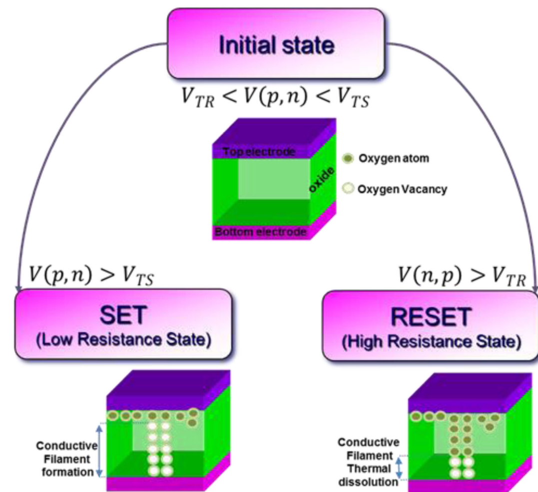

Fig. 3. Schematic representation of the CAMEM model at different RRAM cell states.

A. State Variable

To properly model the I–V characteristic of memristive devices, we use an internal state variable and an implicit differential equation. The state variable w_p is defined as the length of the conducting filament in the memristor device. The evolution rate of w_p due to the growth/rupture of the filament obeys Arrhenius law. The equation defining the state variable evolution (7) uses exponential function replaced by its Taylor series of 6th order within the interval [−1, 1] (6), which is enough to maintain an accuracy of 10^{-3} [21] while reducing the complexity of the model and enhancing the simulation runtime as explained later in Section IV.C.

$$e^x = 1 + x + \frac{x^2}{2!} + \cdots + \frac{x^6}{6!} + R_6(x); \quad R_6(\mathrm{x}) \leq 10^{-3} \tag{6}$$

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TABLE I
CAMEM MODEL PARAMETERS AND DEFINITION

	Param.	Default value	Meaning
Category I defined by the device structure, material properties, and test environment	a	$2.5e^{-9}$	atomic spacing of the switching oxide (m)
	f	$1e^{13}$	vibration frequency of oxygen atom (Hz)
	E_a	0.7	average active energy of Oxygen Vacancy in RESET process (eV)
	E_b	$0.7e^{-6}$	average active energy of Oxygen Vacancy in SET process (eV)
	T_0	300	room temperature (K)
	R_{TH}	$5e^{5}$	thermal resistance (k/W)
Category II consists of parameters that describe the filament evolution	*alpha*	$7.5e^{-13}$	enhancement factor in lower E_a (RESET)
	beta	$7.5e^{-13}$	enhancement factor in lower E_b (SET)
	I_{0S}	$0.5e^{-9}$	hopping current density in the filament region (A/m^2)
	I_{0R}	$0.5e^{-7}$	hopping current density in the gap region (A/m^2)
	V_{TS}	0.1	SET threshold voltage (V)
	V_{TR}	0.1	RESET threshold voltage (V)
	W_{CF}	$5e^{-9}$	Fixed width of the RRAM switching layer (m)
	varCF	$1e^{-4}$	filament radius variation

$$\frac{dw_p}{dt} = \begin{cases} a \times f \times e^{x_s}, & V(p,n) > V_{TS} > 0 \\ a \times f \times e^{x_r}, & V(p,n) < V_{TR} < 0 \\ 0, & V_{TR} < V(p,n) < V_{TS} \end{cases} \tag{7}$$

The parameters x_s and x_r are given in (9):

$$x_s = \frac{E_b - V(p,n) \times \frac{beta}{w_p}}{K_b \times T_{emp}} \text{ and } x_r = \frac{E_a - V(p,n) \times \frac{alpha}{w_p}}{K_b \times T_{emp}} \tag{8}$$

All the other parameters used in (8) and (9) are defined in Table I.

B. Current-Voltage Relationship in the Proposed Model

In addition to the threshold consideration missing in many previously proposed physical models, another critical characteristic of memristor devices is that the switching speed of the SET and RESET phases is different [13], [19]. To the authors' best knowledge, the proposed model is the first physical model presenting different current-voltage relationships (9) for SET and RESET operations, including a different threshold voltage/current for each phase.

$$I_{(p,n)} = \begin{cases} I_S + I_{0s} \times \pi \times \frac{dw_p}{4} \times \sinh\left(\frac{V_{gs}}{V_{TS}}\right), & V(p,n) > V_{TS} > 0 \\ I_R + I_{0R} \times \pi \times \frac{dw_p}{4} \times \sinh\left(\frac{V_{gr}}{V_{TR}}\right), & V(p,n) < V_{TR} < 0 \\ 0, & V_{TR} < V(p,n) < V_{TS} \end{cases} \tag{9}$$

The parameter I_S and I_R are given in (10), where V_{gs} and V_{gr} are two local variables.

$$I_S = I_{0s} \times \pi \times \left(\frac{w_{CF}^2}{4} - \frac{{w_p}^2}{4}\right) \text{ and } I_R = I_{0R} \times \pi \times \left(\frac{{w_p}^2}{4} - \frac{w_{CF}^2}{4}\right) \tag{10}$$

In the I–V relationship previously defined in (10), two main properties of the memristor are modeled. The first terms I_S and I_R (11), using the approximation of exponential function, model a Schottky barrier between the oxide layer and the bottom electrode. The second term, using the approximation of a hyperbolic sine function is due to the tunneling through the MIM junction and models well the characteristics of a memristor for both single and multiple sweeps. As explained in Section III, the hyperbolic sine function is replaced by its Taylor series of 7th order (11), in order to reduce simulation run-time.

$$\sinh(x) = \left(x + \frac{x^3}{3!} + \frac{x^5}{5!} + \frac{x^7}{7!}\right) \tag{11}$$

C. Intrinsic Variability

Variability is one of the main features of RRAM [22]. Compared to other emerging memories, resistive memories provide extensive statistical distributions for different switching parameters such as switching voltage, high-state-resistance (R_{HRS}), and low-state-resistance (R_{LRS}) [22]. This device-to-device variability has a major effect on performance and reliability at the system level. Consequently, variability-aware models are highly recommended. It has been demonstrated recently that variations in R_{HRS} and R_{HRS} are due to random CF formation/rupture. Moreover, the random nature of the ion migration barriers can induce variability of switching voltages [23].

The proposed model can be used in two versions based on a switch variable set by the user.

$$parameter\ real\ var = 1;$$
$$//\ var = 1 : variation\ is\ included$$
$$//\ var = 0 : no\ variation\ included$$

A simplified version without any variation is useful for simulation of the switching behavior at the cell level, and a variability-aware version has a Gaussian sequence added to the CF growth equation (7):

$$random_cf_var = \$rdist_normal\ (rand_set_var, 0, 1) * varCF \tag{12}$$

D. Model Parameters

For a compact model, it is critically important to have a clear procedure to extract model parameters [24]. Such parameters are divided into two categories, as defined in Table I. The default values represent reasonable values based on experimental data and physical insights from different memristor devices [9], [10], [30].

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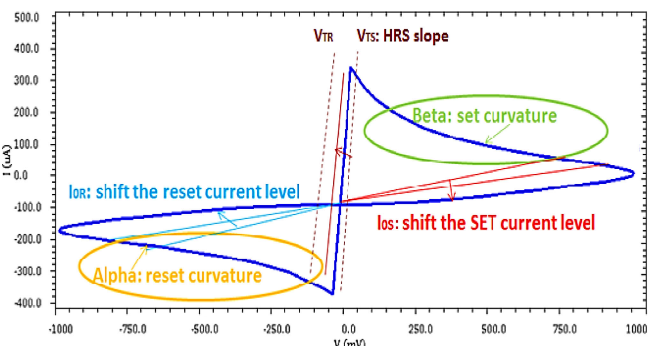

Fig. 4. Summary of the impacts of the different model parameters.

The I–V characteristic of the proposed model is presented in Fig. 4. The effect of each parameter is analyzed while maintaining other parameters fixed.

The set of parameters, *Alpha, Beta,* I_{0S}, I_{0R}, V_{TS}, and V_{TR} describes the filament evolution. *Alpha* and *beta* mainly change the RESET and SET curvatures, respectively; while I_{0S} and I_{0R} shift the SET/RESET current levels. V_{TS} captures the SET threshold voltage and the slope of the HRS (High Resistance State or OFF state). V_{TR} captures the RESET threshold voltage and the slope of the LRS (Low Resistance State or ON state). An accurate estimation of these parameters can be extracted from the median switching curve of the experimental data.

In the CAMEM model, the state variable w_p is a physical parameter showing the evolution of the conductive filament within the interval $[0, W_{CF}]$ where W_{CF} is the fixed width of the RRAM switching layer. The state variable assumes symmetric switching behavior if the initial currents I_S and I_R have the same values.

IV. Validation of the CAMEM Model

We opted for a Verilog-A implementation of the proposed model, rather than a SPICE macro-model since it requires less computational time while maintaining similar accuracy [17].

The choice of the applied signal frequency is also critical for reliable memristor switching. If the period of the applied signal does not exceed the SET/RESET switching time, then the memristor would be in an intermediate state rather than entirely switched to HRS or LRS. The memristor devices considered in this section have a switching time in the microsecond regime.

Therefore, based on this high-speed feature, this model can be used to simulate accurately neuromorphic systems, RRAM memories …

A. Transient, DC and AC Simulations

To perform a transient analysis, we applied a square signal of 1 V amplitude and 1 MHz frequency across the memory cell. Fig. 5 depicts the obtained transient I–V characteristic of the proposed model. The default values of the model parameters listed in Table I are used. For the given fitting parameters, the main characteristics of the memristor are then measured and presented in Table II. T_{SET}/T_{RESET} is the time needed to set/reset the device, R_{ON} is the low-state resistance, R_{OFF} is the high-state resistance, I_{ON} is the SET phase current, and I_{OFF} is the RESET phase current.

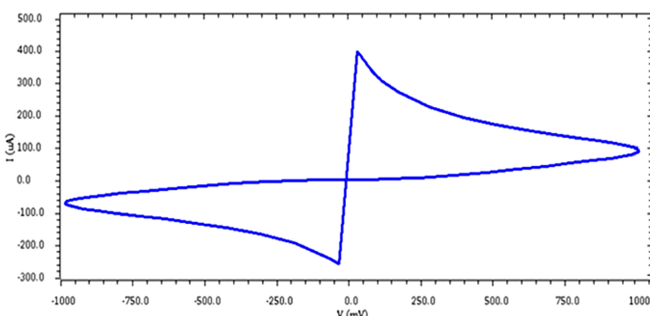

Fig. 5. Simulated transient I–V characteristics of the proposed model.

TABLE II
CAMEM Model Measured Parameters

T_{SET} (ns)	R_{ON} (KΩ)	I_{ON} (uA)	T_{RESET} (ns)	R_{OFF} (KΩ)	I_{OFF} (uA)
0.675	1.32	757	1.2	34.48	29

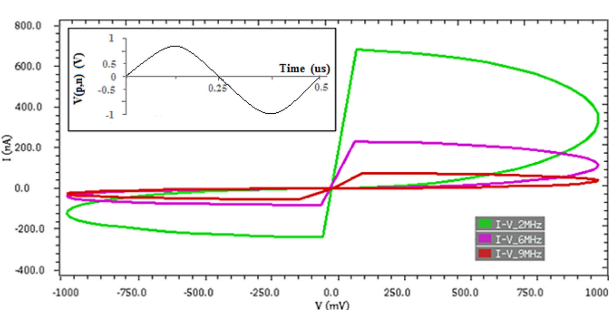

Fig. 6. I–V characteristics of the proposed model at different frequencies.

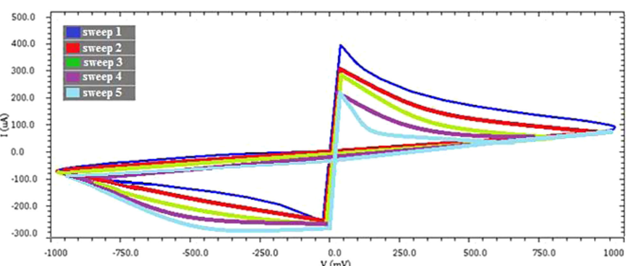

Fig. 7. CAMEM model I–V characteristics for 5 consecutive DC sweeps.

Fig. 6 shows the frequency effect on the I–V characteristic. A sine wave *V(p, n)* of different frequencies (2 MHz, 6 MHz, and 9 MHz), is applied in order to simulate the effect of the frequency on the proposed model I–V characteristic. As evident from Fig. 6, as the frequency increases, the memristive effect is considerably reduced. The memristor I–V hysteresis curve is deteriorated (narrower) since the device does not have enough time to switch its resistance state when biased.

Fig. 7 represents the I–V characteristics for five consecutive DC voltage sweeps. All DC sweep measurements consist of a

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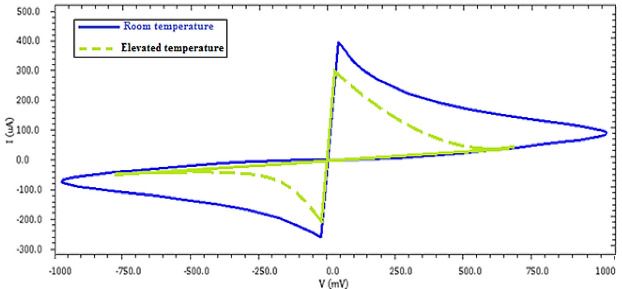

Fig. 8. Simulation of thermal effects in the CAMEM model.

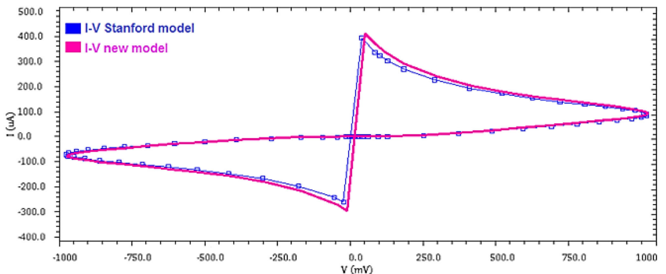

Fig. 9. CAMEM fitted to the Stanford model: I–V curve for both models.

SET/RESET/SET sequence, where SET corresponds to a 0 to 1 V voltage sweep, and RESET corresponds to a 0 to –1 V voltage sweep. Fig. 7 shows that the size of the hysteresis loops decreases when the conductivity of the device increases as predicted from the I–V equations (9) and (10). Subsequent I–V curves incorporate changes in the currents (I_S and I_R) arising from residual filaments remaining after the completion of previous cycles. As such, we demonstrated that the proposed model works consistently in different analyses under time, voltage, and frequency variations.

B. Thermal Effect Analysis

The proposed model can also account for the thermal effect, modeled by the change in the *I–V* characteristics as a function of the temperature.

When the resistive switching occurs, the CF temperature performs a significant effect [25] in accelerating the process included in equations (7) and (9). The temperature of the conductive filament, presented in (13), is directly modified by the Joule-heating effect.

$$T_{\text{emp}} = T_0 + I\left(p,n\right) \times V\left(p,n\right) \times R_{th} \quad (13)$$

Parameters T_0 and R_{th} are respectively, the ambient temperature and the thermal resistance of the CF. The thermal resistance effect introduced in [26] to simplify the differential equation for the Joule heating temperature traditionally used in the literature. The temperature T_{emp} affects the filament growth directly through (7) and (9).

Following the previous assumption, increased temperature decreases the current required for SET and RESET switching, as shown in Fig. 8.

C. Fitting the CAMEM Model to a Reference Model

We performed a comparison in terms of accuracy and complexity with a reference model (Stanford model) to demonstrate the proposed model's effectiveness. We use the relative root mean squared error to fit the I–V curve:

$$RMS_{I,V} = \sqrt{\frac{\sum_{k=1}^{n}\left(\text{Vx} - \text{Vref, x}\right)^2}{n \parallel \text{Vref}\|^2} + \frac{\sum_{k=1}^{n}\left(\text{Ix} - \text{Iref, x}\right)^2}{n \parallel \text{Iref}\|^2}} \quad (14)$$

TABLE III
FITTING ACCURACY AND RUNTIME IMPROVEMENT

Mean I-V error (%)	**1.42**
Maximum I-V error (%)	**11.2**
Simulation runtime improvement (%)	**47.06**

TABLE IV
CAMEM MODEL FITTING PARAMETERS USED

E_a = 0.4	E_b = 0.7	a = 2.5e-9	f = 1e+13
R_{TH} = 500000	T_0 = 300	*alpha* = 7.5e-15	*beta* = 7.5e-10
$I_{0\text{S}}$ = 0.5e-7	$I_{0\text{R}}$ = 3.5e-8	V_{TS} = 0.001	V_{TR} = 0.001

In this equation, *n* is the sample number, V/I are the corresponding voltage and current of the CAMEM model, V_{ref}/I_{ref} are the corresponding voltage and current of the reference model and $\parallel Vref \parallel$ / $\parallel Iref \parallel$ are respectively, the Euclidean norm of the voltage and current of the reference model.

The fitting procedure is iterated on *alpha* and *beta* to minimize the relative root mean squared error given in (14). The other fitting parameters (i.e., I_{0S}, I_{0R}, V_{TS}, and V_{TR}) are manually set. As shown in Fig. 9, an excellent agreement between the two models is obtained (RMS error less than 2%).

When using the proposed model, the simulation runtime can be enhanced by around 47%, and the accuracy remains sufficient with a mean error of 1.42%. The results presented in Table III depend on the model parameters. The fitting parameters used to perform this comparison are listed in Table IV.

The simulation runtime efficiency of the proposed model is mainly due to the reduced function calls since Taylor polynomials replaced the complex functions. The efficiency of this method has been demonstrated in [27]. However, additional efficiency tests should be performed in future work to cover larger memristor arrays and emerging RRAM architectures such as the crossbar [28] and the 3D vertical arrays modeling [29].

D. Model Validation at the Array Level

In the previous sections, we have exhaustively evaluated the dynamic behavior of the proposed model at a single RRAM cell level. Nevertheless, in order to validate the model at the circuit level, the model functionality has been evaluated by simulating numerous RRAM cells connected in a 1T1R memory array. For our analysis, we use a 1K-bit RRAM array to keep a reasonable simulation time and get significant results at the same time. The complete simulated memory array is shown in Fig. 10. First,

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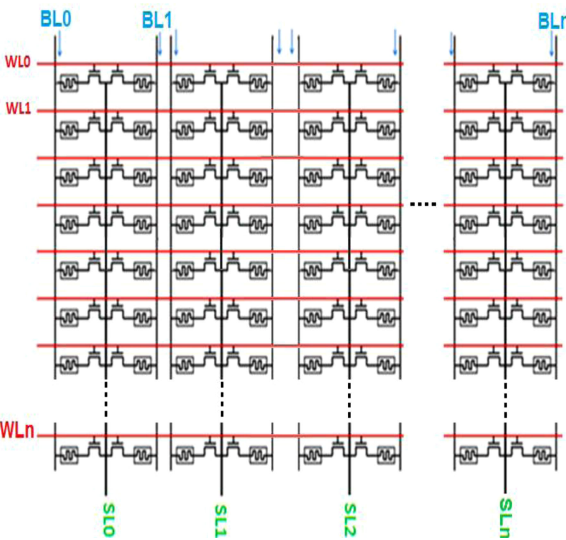

Fig. 10. Schematic of the simulated 1T1R memory array (n = 1 K).

TABLE V
CAMEM MODEL SIMULATION EFFICIENCY FOR 1 K-BIT ARRAY

Model	Simulation run time (s)	Computation memory (MB)
Stanford [10]	46.47	538
CAMEM Model	29.14	532

all the RRAM cells are RESET (set to high resistance state). Then, two cycles are required to perform the programming of the memory array. First, all memory cells are set (logical “1”), then the memory array is reset (logical “0”). Simulation results are consistent with those of single-cell operation.

An additional critical concern when using the RRAM model for simulations of large arrays is the enormous computing resources required. Table V gives the simulation run time and the computation memory usage for the proposed model compared to the Stanford model using a main memory of 26 GB for a 64-core Intel(R) Xeon(R) (CPU E5-2680 v2 @ 2.80 GHz) server.

V. EXPERIMENTAL VERIFICATION

We calibrated the CAMEM model on recent electrical data measured on HfO2-based OxRAM devices provided by ST microelectronics [30] to validate the theoretical approach used in Section III. In this study, the memory elements consisted of a Ti/HfO_2/TiN stack with a 5 nm thick hafnium oxide.

The graphical results of the I–V relationships depicted in Fig. 11 prove that the proposed model accurately fits the experimental data in both SET and RESET phases. The CAMEM model captures well the ‘hard’ set, and ‘soft’ reset behavior of the actual memristive device.

A B1500 semiconductor parameter analyzer is used for measurements. Quasi-static experimental measurements are performed to extract the memory cell main characteristics (i.e., V_{SET}, V_{RESET} ...) by applying a 200 ms triangular pulses across the 1T1R cell. The simulation of the proposed model

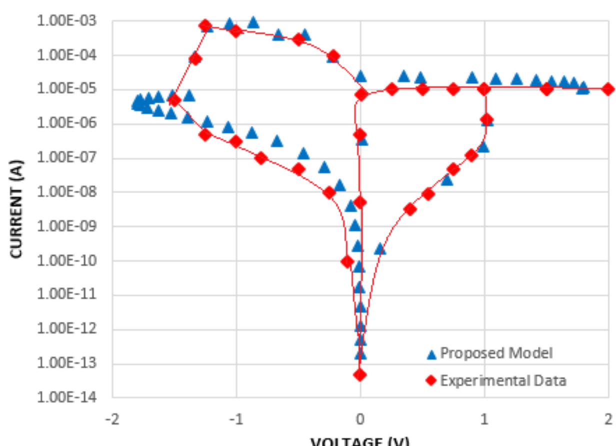

Fig. 11. Proposed model fitted to experimental data [30]. Fitting parameters: $E_a = 0.3$, $E_b = 0.3$, alpha $= 7.5e^{-10}$, beta $= 7.5e^{-6}$, $I_{0S} = 0.5e^{-8}$, $I_{0R} = 3.5e^{-9}$, $V_{TS} = 0.005$, $V_{TR} = 0.01$.

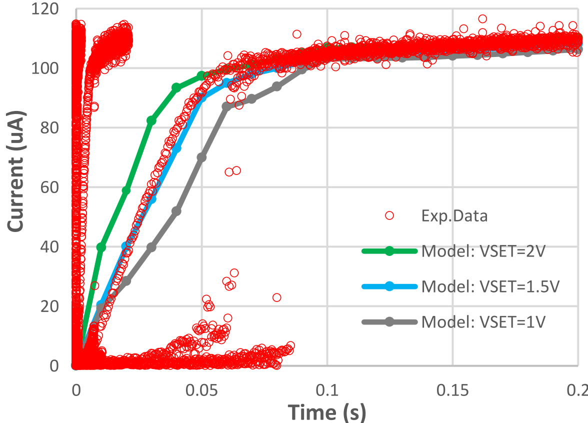

Fig. 12. SET current response together with experimental data [30].

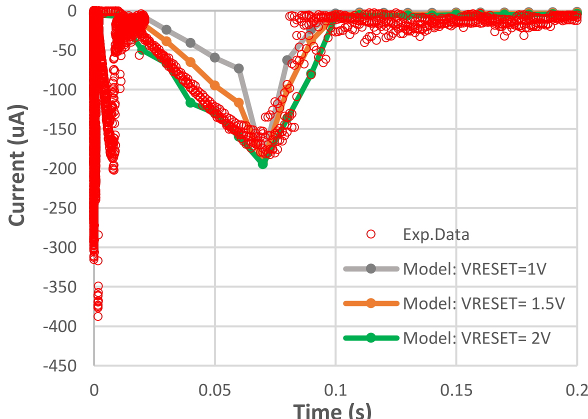

Fig. 13. RESET current response together with experimental data [30].

is performed using the same pulse programming condition as the measured data. Fig. 12 and Fig. 13 show an excellent agreement between the transient current response during SET and RESET phases at different voltages and the experimental data. This proves that the CAMEM model captures very well the quasi-static current responses as the actual memristor.

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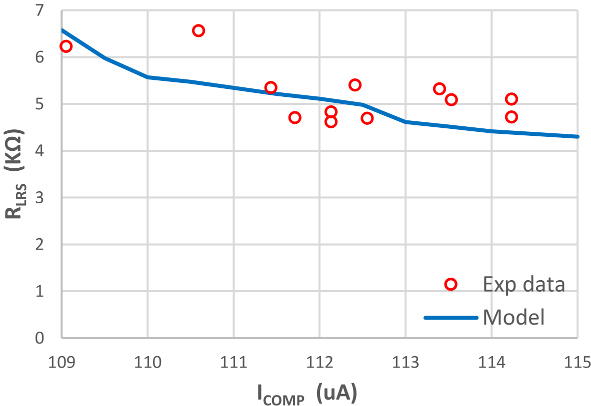

Fig. 14. Measured and simulated RLRS under different compliance currents.

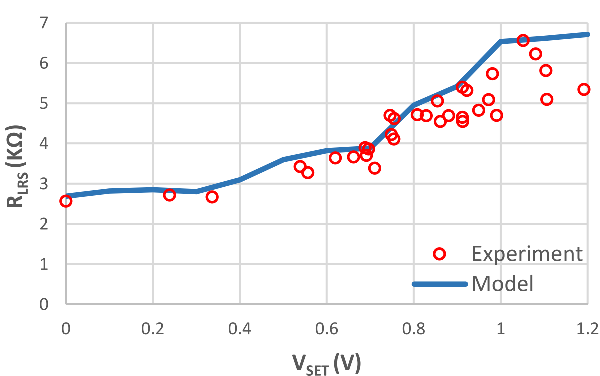

Fig. 15. Measured and simulated RLRS under different SET voltages.

In the proposed model, a lateral CF growth process during SET is also assumed. Figs. 14 and 15 present the validation of this assumption. In Fig. 14, the variation of R_{LRS}, as a function of compliance current during SET, is simulated and compared to the experimental data. When the compliance current increases, it lowers the R_{LRS}, and hence, a larger CF is built. Fig. 13 shows also that R_{LRS} is very sensitive to any change in the compliance current: a standard deviation of 0.62 of R_{LRS} values is observed in a small range of 6 uA.

Fig. 15 shows that R_{LRS} is increasing rapidly with the SET voltage leading to an 'abrupt' SET; this observation is in agreement with the physics aspect of the actual memristive device. Indeed, during the SET process, the width of the CF increases, and hence the temperature increases, speeding up the reaction.

Similarly, the 'gradual' RESET is well captured by the model, as shown in Fig. 16. In fact, during the RESET process, the width of the CF decreases, and hence the temperature decreases, slowing down the reaction.

The intrinsic variability included in the CAMEM model (13) is tested and compared to the experimental results. Fig. 17 presents the cumulative distributions of the LRS and HRS resistances of the model and the actual memristive device over consecutive sweeps. The CAMEM model simulated data (blue lines) is consistent with experimental data (red symbols). In general, for oxide-based memristors, variability is more extensive in HRS than LRS. As demonstrated above, LRS is controlled by the compliance current.

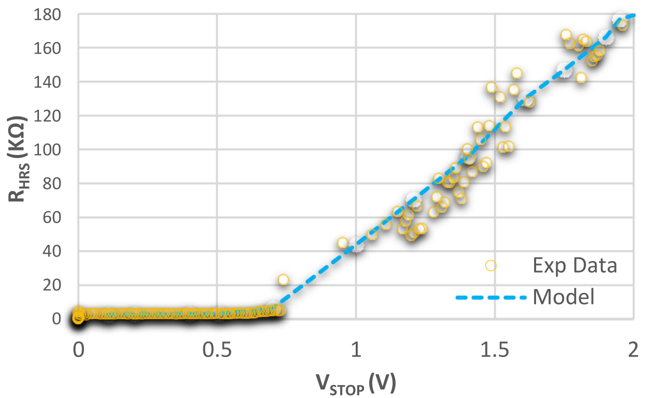

Fig. 16. Measured and simulated RLRS under different SET voltages.

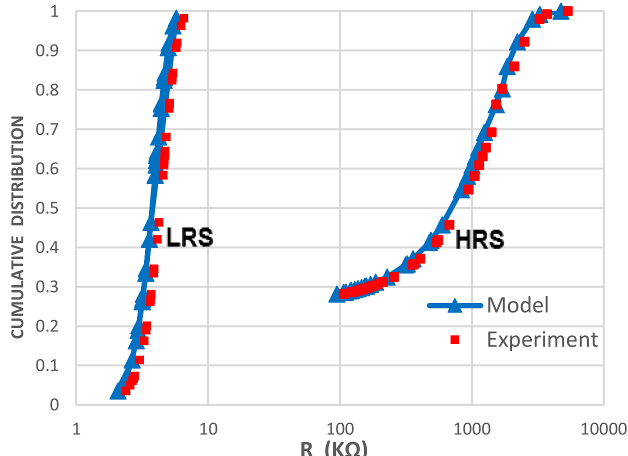

Fig. 17. Cumulative distributions of RHRS and RLRS.

VI. Conclusion

The paper presents a novel Verilog-A compact model, including the most noticeable physics of actual memristor devices such as the conductive filament growth/rupture, threshold voltage/current, temperature dependency, and variability. Moreover, the proposed model captures very well the transient, DC, and AC programming current. By performing different simulations and validation with experimental data (5 nm thick hafnium oxide Ti/HfO_2/TiN), we demonstrated also that the CAMEM model is flexible, generic, sufficiently accurate, and computationally efficient compared to existing memristor models and hence, it can be easily used for simulations at the circuit level to guide the designers in several applications that involve different types of memristors.

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